

### 3.8 A BJT-Based CMOS Temperature Sensor Achieving an Inaccuracy of $\pm 0.45^\circ\text{C}$ ( $3\sigma$ ) from $-50^\circ\text{C}$ to $180^\circ\text{C}$ and a Resolution-FoM of $7.2\text{pJ}\cdot\text{K}^2$ at $150^\circ\text{C}$

Bo Wang<sup>1</sup>, Man-Kay Law<sup>2</sup>, Amine Bermak<sup>1</sup>

<sup>1</sup>Hamad Bin Khalifa University, Doha, Qatar

<sup>2</sup>University of Macau, Macau, China

Integrated temperature sensors for industrial digital transformation such as turbine and bearing monitoring should exhibit low power consumption and high energy efficiency with moderate inaccuracy over a wide sensing range (e.g.,  $>150^\circ\text{C}$ ) to achieve autonomous operation under a limited energy budget. Even though resistor-based temperature sensors can achieve a superior sub-pJ-K<sup>2</sup> resolution-FoM [1], they typically require a 2-point trim together with a high-order nonlinearity correction (6<sup>th</sup>-order in [2]), inevitably burdening the processing cost. In contrast, BJT-based temperature sensors in bulk or SOI CMOS can achieve accurate sensing at high temperature with only 1-point trim and simple digital processing [3,4]. However, they can suffer from a degraded energy efficiency at high temperature for ensuring the sensing resolution and/or accuracy (e.g.,  $\sim 3\times$  increase in bias current for improving the  $3\sigma$ -inaccuracy from  $\pm 0.6^\circ\text{C}$  to  $\pm 0.4^\circ\text{C}$  in [3]). This paper describes a BJT-based temperature sensor capable of wide-range operation from  $-50^\circ\text{C}$  to  $180^\circ\text{C}$ . By employing a nonlinear readout and the proposed sub-ranging, double-sampling, and constant-biasing techniques, this work achieves a high resolution-FoM over the entire sensing range ( $9.7\text{pJ}\cdot\text{K}^2$  at room temperature and  $7.2\text{pJ}\cdot\text{K}^2$  at  $150^\circ\text{C}$ ), corresponding to a 6-to-10 $\times$  improvement when compared with prior BJT-based wide-range designs [3,4]. We further employ dynamic error-correction [5] and switch-leakage compensation to effectively suppress the mismatch- and leakage-induced errors, resulting in a high precision of  $\pm 0.45^\circ\text{C}$  ( $3\sigma$ ).

Figure 3.8.1 depicts the system diagram of the proposed CMOS temperature sensor, consisting of a BJT-core, a switched-capacitor (SC)  $\Delta\Sigma$ -ADC, and a digital controller. Instead of using a proportional-to-absolute-temperature (PTAT) current that can double the sensor's power consumption from  $-50^\circ\text{C}$  to  $180^\circ\text{C}$ , we only devote the beta-cancellation circuit for BJT biasing, while employing a temperature-compensated peaking current source (total  $0.26\mu\text{A}$ ) for system use. The dominant noise source from the beta-cancellation circuit, which mostly appears at the  $V_{\text{BE0,1}}$  output as a common-mode noise, can only be suppressed during  $\Delta V_{\text{BE}}$  sampling but not when sampling  $V_{\text{BE0}}$ . Consequently, unlike the readout schemes in [3,6], we employ a nonlinear readout scheme with  $X_T = k \cdot \Delta V_{\text{BE}} / V_{\text{BE0}}$ , which effectively reduces the number of  $V_{\text{BE0}}$  samples per conversion while relaxing the resolution requirement at high temperature. Specifically, for a target resolution of  $15\text{m}^\circ\text{C}$ , this nonlinear readout should achieve a 16-bit effective noise level (referenced to  $V_{\text{BE0}}$ ) at  $-50^\circ\text{C}$ , which reduces to only 13.5-bit at  $180^\circ\text{C}$ . To optimize the energy efficiency over the entire sensing range, this work performs sub-ranging using  $k_1=6$  at low temperature (low-T) and  $k_2=3$  at high temperature (high-T), with consideration of both the ADC's maximum stable amplitude ( $<0.8$ ) and a transition temperature of  $T_r \sim 100^\circ\text{C}$ . As a result, it can relax the required ADC input-referred noise power by a factor of 4 and 2.5 in the two subranges, respectively. Using two gains ( $k_1, k_2$ ) does not affect the linearized sensor output  $\mu_T = \alpha / (\alpha + k/X_T)$  as the ratio  $k_1/k_2$  can be precisely defined at room temperature (RT) by converting the same temperature twice with different gain settings ( $k_1/k_2 = X_{T1}/X_{T2}$ ), thus still allowing 1-point  $\alpha$ -trim to compensate for the  $V_{\text{BE0}}$  spread. In addition, we employ double sampling with a single DAC to further improve the sensor energy efficiency by  $2\times$ .

Figure 3.8.2 shows the implementation of beta-cancellation biasing [4] with dynamic error-correction [5] in the sensor front-end. We employ small PNP BJTs ( $2\mu\text{m} \times 2\mu\text{m}$ ) to maintain a high linearity in  $V_{\text{BE0,1}}$  ( $<0.05^\circ\text{C}$  error over full range) with a moderate emitter bias current of  $I_{\text{PT}}=150\text{nA}$  at RT. The 94dB-gain folded-cascade error amplifier ( $A_E$ ) consumes  $0.45\mu\text{A}$ , with its offset and  $1/f$  noise up-modulated by chopping ( $f_{\text{cb}}=f_s/36$ ). The four-wire connections at the BJT outputs prevent accuracy degradation in  $V_{\text{BE0,1}}$  due to the varied voltage drop across the DEM switches (transmission gates). To suppress the switch-leakage-induced nonlinearity in  $V_{\text{BE0,1}}$  at high-T (body-leakage dominant), the PMOS drain/source diffusion area is  $3.6\times$  larger than that of the NMOS to achieve a 1<sup>st</sup>-order body-leakage compensation. Diffusion areas of a switch pair are shared whenever possible to further reduce the body leakage. This results in a measured average leakage reduction of a transmission-gate pair from  $640\text{pA}$  to  $190\text{pA}$  at  $180^\circ\text{C}$ , corresponding to a  $<0.1^\circ\text{C}$  overall linearity error in  $V_{\text{BE0,1}}$ .

Figure 3.8.3 shows the sensor readout with a 2<sup>nd</sup>-order feedforward double-sampled  $\Delta\Sigma$ -ADC. The two sampling paths consisting of  $C_{s1,2}$  ( $C_{s1}=C_{s2}$ ) operate at  $f_s=40\text{kHz}$ , with the 1-bit quantizer clocked at  $2 \cdot f_s$ . When the output bitstream (BS) is high, either one of the  $\Phi_{1d,1dd,2d,2dd}$  falling edges triggers the feedback DAC consisting of  $C_{\text{fb}}$  for charge-balancing, depending on the active sampling path and the current DAC state. This feedback control as triggered by different clock edges can minimize signal-dependent errors introduced

by the DAC. The use of only one DAC feedback path also avoids quantization-noise folding due to DAC mismatch. The varying common-mode voltages for  $V_{\text{BE0}}$  or  $\Delta V_{\text{BE}}$  sampling are canceled by shorting the respective sampling plates of  $C_{s1,s2/\text{fb}}$  during charge redistribution. To implement  $k_1=6$  and  $k_2=3$  while achieving the target resolution, we size  $C_{s1,s2}/C_{\text{fb}}$  to be  $6C_u/1C_u$  and  $12C_u/4C_u$  (with a unit capacitance  $C_u=260\text{fF}$ ) in the two subranges, respectively. The 1<sup>st</sup>-integrator gain is set to  $1/3$  ( $C_{\text{int1}}=3C_u/12C_u$  in the two subranges) to balance the thermal noise contribution between the front-end and the ADC. Sub-ranging decision is achieved by checking the polarity of  $6 \cdot (8\Delta V_{\text{BE}} - V_{\text{BE0}})$ , in which the  $6\times$  gain can reduce the  $T_r$  variations as induced by the comparator offset. The sensor then runs for  $162 \Delta\Sigma$  cycles ( $324$  output bits). System-level chopping ( $f_{\text{sys}}$ , once per conversion) suppresses the residue  $1/f$  noise by inverting the input polarity and averaging the decimated output.

The 1<sup>st</sup> integrator in Fig. 3.8.3 consists of two  $\sim 80\text{dB}$ -gain chopped current-reuse amplifier slices ( $A_{1,2}$ ) with different transistor bias conditions to maximize their respective output swings in the two subranges while consuming  $0.8\mu\text{A}$  and  $1.65\mu\text{A}$ , respectively. Despite the reduced settling requirement,  $A_{1,2}$  designed for the high-T range consumes more power due to the  $2\times$  larger  $C_s$  and the degraded transistor  $g_m/I_d$  efficiency. The 2<sup>nd</sup>-integrator, which has a much-relaxed noise requirement, draws  $170\text{nA}$ , and is bypassed during the subrange decision phase. We employ T-switches [4] with body-leakage compensation in the sensor readout to minimize its influence on  $V_{\text{BE0,1}}$  during sampling. Notice that applying the conventional DEM to  $C_{s1,s2,\text{fb}}$  requires a total of 336 switches for the 56 unit capacitors. Consequently, as the ratio  $k_1/k_2$  can be determined at RT, we just perform a local DEM at low-T by involving all unit capacitors of  $C_{s1,s2,\text{fb}}$  within one conversion to minimize the spread of  $k_1$  and the layout-dependent ratio error of  $k_1/k_2$ . The DEM of  $C_{\text{fb}}$  is controlled by BS to ensure all unit capacitors can equally contribute to the feedback operation, at the cost of a small temperature-dependent noise tone in the BS output.

This  $0.42\text{mm}^2$  sensor was fabricated in a standard  $0.18\mu\text{m}$  CMOS process. The die micrograph is shown in Fig.3.8.7. We implement the sinc<sup>3</sup> decimation filter off-chip for testing flexibility. Clocked at  $40\text{kHz}$ , the sensor employs a customized clock-gated digital controller using HVT devices, drawing  $2.5\mu\text{A}$  at RT, and  $3.8\mu\text{A}$  at  $150^\circ\text{C}$  from a  $1.5\text{V}$  supply. The current consumption further increases to  $5.7\mu\text{A}$  ( $\sim 2\mu\text{A}$  from digital) at  $180^\circ\text{C}$ . Figure 3.8.4 shows the sensor output PSD, indicating a suppressed  $1/f$  noise corner of  $<150\text{mHz}$ . With dynamic error correction, the best achieved kT/C-limited resolution is  $17.6\text{mK}_{\text{rms}}$  (with local DEM enabled) under a conversion time of  $8.325\text{ms}$  at RT, corresponding to a resolution-FoM of  $9.7\text{pJ}\cdot\text{K}^2$ . By exploiting a nonlinear readout, sub-ranging technique, double sampling, and constant-biasing method, this work further demonstrates a resolution-FoM of  $7.2\text{pJ}\cdot\text{K}^2$  at  $150^\circ\text{C}$ . The measured supply sensitivity is  $0.44^\circ\text{C}/\text{V}$  from  $1.5\text{V}$  to  $2\text{V}$ . Figure 3.8.5 presents the measured performance with a total of 25 samples from  $-50^\circ\text{C}$  to  $180^\circ\text{C}$ . Note that hysteresis around  $T_r$  (the transition region) will not affect the temperature reconstruction. As observed, the untrimmed inaccuracy is  $\pm 1.8^\circ\text{C}$  ( $3\sigma$ ). After 1-point  $\alpha$ -trim and  $k_1/k_2$  ratio correction at RT, the inaccuracy improves to  $\pm 0.45^\circ\text{C}$  ( $3\sigma$ ), ultimately limited by process spreads instead of nonlinearity at high-T. Figure 3.8.6 benchmarks this work with the state-of-the-art wide-range smart temperature sensors. Except from the resistor-based design [1], which requires high-order nonlinearity cancellation, this work in bulk CMOS achieves a 6-to-10 $\times$  higher energy efficiency than prior BJT-based works [3,4] with comparable sensing resolution and trimming effort.

#### Acknowledgement:

This work was sponsored by the NPRP grant NPRP11S-0104-180192 from the Qatar National Research Fund.

#### References:

- [1] K. A. A. Makinwa, "Smart Temperature Sensor Survey", [Online]. Available: [http://ei.ewi.tudelft.nl/docs/TSensor\\_survey.xls](http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls)
- [2] S. Pan et al., "A  $0.12\text{mm}^2$  Wien-Bridge Temperature Sensor with  $0.1^\circ\text{C}$  ( $3\sigma$ ) Inaccuracy from  $-40^\circ\text{C}$  to  $180^\circ\text{C}$ ," *ISSCC*, pp. 184-186, Feb. 2019.
- [3] K. Souri et al., "A  $40\mu\text{W}$  CMOS Temperature Sensor with an Inaccuracy of  $\pm 0.4^\circ\text{C}$  ( $3\sigma$ ) from  $-55^\circ\text{C}$  to  $200^\circ\text{C}$ ," *ESSCIRC*, pp. 221-224, Sept. 2013.
- [4] B. Yousefzadeh et al., "A BJT-Based Temperature-to-Digital Converter with a  $\pm 0.25^\circ\text{C}$   $3\sigma$ -Inaccuracy from  $-40^\circ\text{C}$  to  $+180^\circ\text{C}$  Using Heater-Assisted Voltage Calibration," *IEEE JSSC*, vol. 55, no. 2, pp. 369-377, Feb. 2020.
- [5] Y. Hsu et al., "An  $18.75\mu\text{W}$  Dynamic-Distributing-Bias Temperature Sensor with  $0.87^\circ\text{C}$  ( $3\sigma$ ) Untrimmed Inaccuracy and  $0.00946\text{mm}^2$  Area," *ISSCC*, pp. 102-103, Feb. 2017.
- [6] S. H. Shalmany et al., "A Micropower Battery Current Sensor with  $\pm 0.03\%$  ( $3\sigma$ ) Inaccuracy from  $-40$  to  $+85^\circ\text{C}$ ," *ISSCC*, pp. 386-387, Feb. 2013.

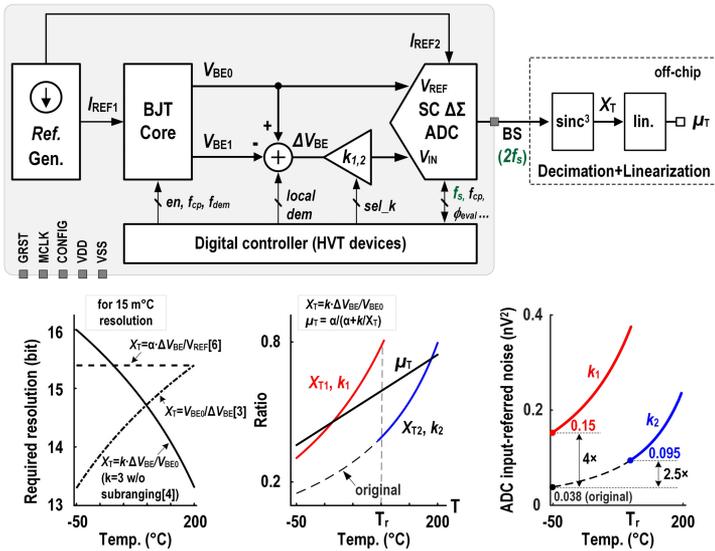


Figure 3.8.1: Proposed sub-ranging temperature sensor with double-sampled SC ΔΣ-ADC for wide-range operation and energy-efficiency optimization.

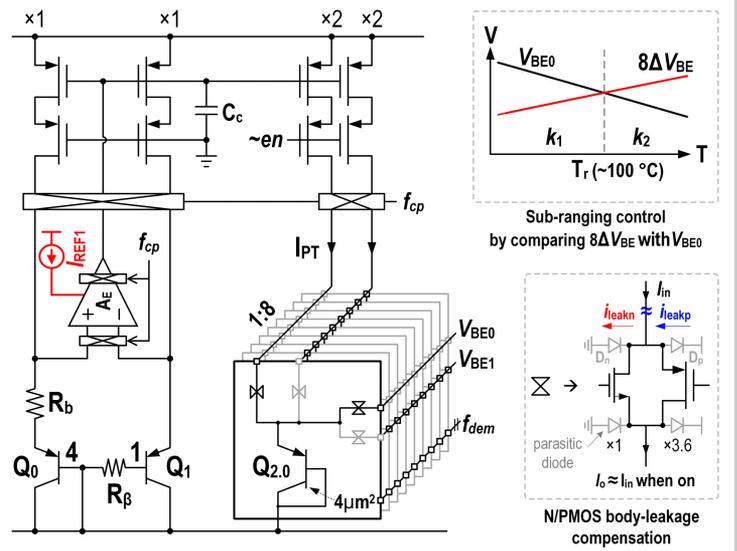


Figure 3.8.2: Sensor front-end with four-wire BJT output connection and switch body-leakage compensation to maintain signal linearity at high temperatures.

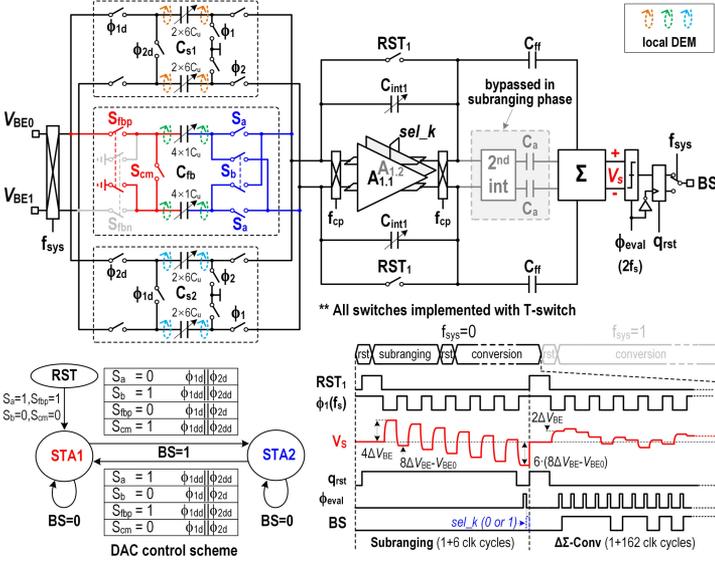


Figure 3.8.3: Double-sampled ΔΣ-ADC using a single DAC and with local DEM to reduce  $k_1/k_2$  spread (top); DAC control and readout timing at  $f_{sys}=0$  (bottom).

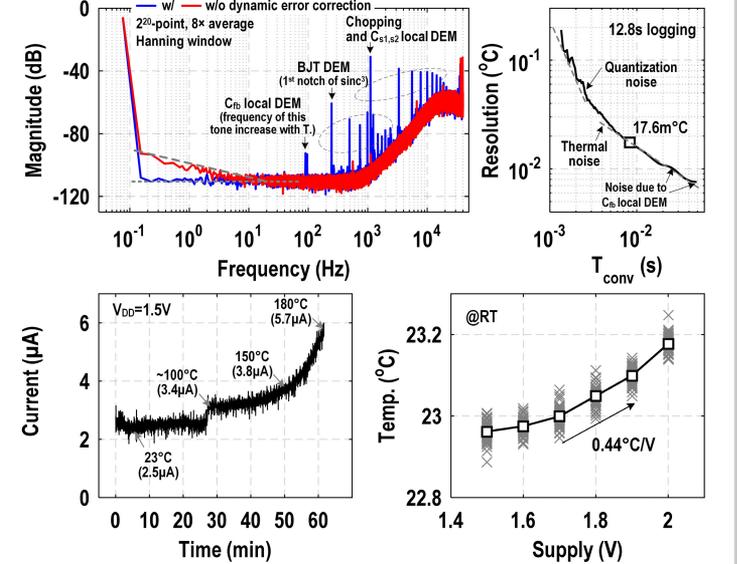


Figure 3.8.4: PSD of the output BS and resolution over time (top); logged sensor current with increasing ambient temperature and supply sensitivity (bottom).

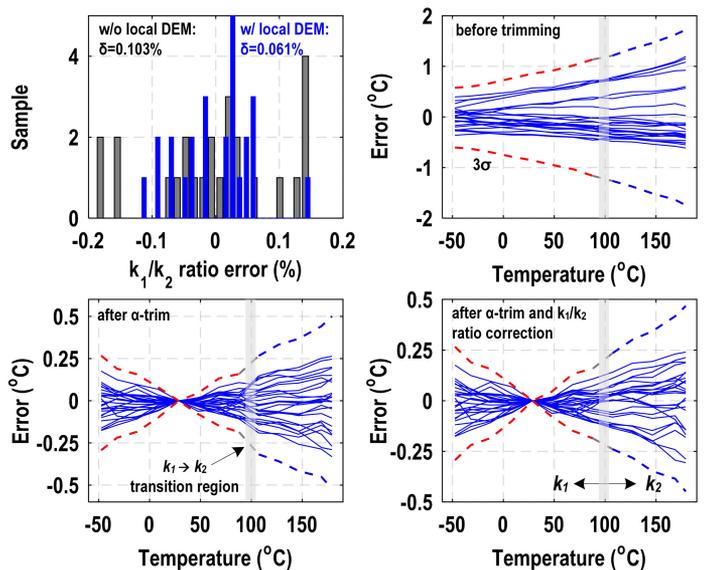


Figure 3.8.5: Measured  $k_1/k_2$  spread and untrimmed temperature error (top); error after  $\alpha$ -trim and both  $\alpha$ -trim and  $k_1/k_2$  ratio correction (bottom).

	ISSCC'19 [2]	ESSCIRC'13 [3]	JSSC'20 [4]	ISSCC'17 [5]	This work
Technology	0.18 $\mu\text{m}$	0.16 $\mu\text{m}$ SOI	0.16 $\mu\text{m}$	28 nm	0.18 $\mu\text{m}$
Sensor Type	Resistor	BJT	BJT	BJT	BJT
Area	0.12 $\text{mm}^2$	0.1 $\text{mm}^2$	0.15 $\text{mm}^2$	0.01 $\text{mm}^2$	0.42 $\text{mm}^2$
Samples	20	7	24	76	25
Supply Voltage	1.8 V	1.6 ~ 2 V	1.8 V	1.8 V	1.5 ~ 2 V
Sensing Range	-40 °C to 180 °C	-55 °C to 200 °C	-40 °C to 180 °C	-25 °C to 125 °C	-50 °C to 180 °C
3 $\sigma$ Inaccuracy (Trim points)	$\pm 0.4$ °C (1-pt) <sup>a</sup> $\pm 0.11$ °C (2-pt) <sup>a</sup>	$\pm 0.4$ °C (1-pt)	$\pm 0.2$ °C (1-pt) $\pm 0.25$ °C (vcal)	$\pm 1.85$ °C (0-pt)	$\pm 1.8$ °C (0-pt) $\pm 0.45$ °C (1-pt)
Relative Inaccuracy <sup>b</sup>	0.36% (1-pt) 0.1% (2-pt)	0.31% (1-pt)	0.18% (1-pt) 0.23% (vcal)	2.47% (0-pt)	1.57% (0-pt) 0.39% (1-pt)
T <sub>conv</sub>	10 ms	4.2 ms	20 ms	8.2 ms	8.3 ms
Power (at RT)	52 $\mu\text{W}$	35.2 $\mu\text{W}$	9.8 $\mu\text{W}$	18.8 $\mu\text{W}$	RT: 3.8 $\mu\text{W}$ 150 °C: 5.7 $\mu\text{W}$
Resolution	0.46 m°C	20 m°C	23 m°C	150 m°C	17.6 m°C 12.3 m°C
Res. FoM <sup>c</sup>	0.1 pJ-K <sup>2</sup>	59 pJ-K <sup>2</sup>	103 pJ-K <sup>2</sup>	3500 pJ-K <sup>2</sup>	9.7 pJ-K <sup>2</sup> 7.2 pJ-K <sup>2</sup>

a: 6<sup>th</sup>-order nonlinearity removal  
 b: Relative inaccuracy (%) = Max error / specified sensing range  $\times 100$   
 c: Res. FoM = Energy/Conversion  $\times$  Resolution<sup>2</sup>

Figure 3.8.6: Performance summary and benchmark with state of the art.

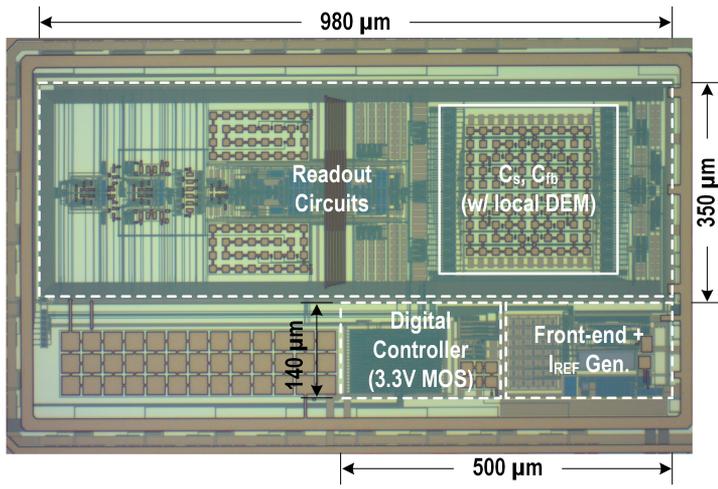


Figure 3.8.7: Die micrograph of the designed temperature sensor in 0.18μm 1.8/3.3V 1P6M CMOS process.