# On Fully Differential Incremental $\Delta\Sigma$ ADC With Initial Feedback Zeroing and 1.5-Bit Feedback

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***Abstract*—This paper presents the time-domain analysis of a fully differential incremental $\Delta\Sigma$ modulator. Particularly, the influence of the bipolar feedback signal on the quantization noise of the modulator is analyzed, which is overlooked in most IDC designs. Based on the analysis, an initial feedback zeroing scheme is introduced to decrease the quantization noise of the modulator. Moreover, the maximum number of output codeword that can be produced by the modulator is mathematically derived. Following the derivation, a control scheme is proposed to achieve 1.5-bit effective feedback without changing the quantizer and D/A topology. By applying the initial feedback zeroing and 1.5-bit feedback technique, quantization noise of the 1st- and 2nd-order modulators analyzed in this paper can be decreased by 4×, with very minor modifications on the modulator's original digital controllers.**

***Index Terms*—incremental delta-sigma analog-to-digital converter, fully differential IDC, 1.5-bit feedback, modulator codeword, time-domain analysis**

## I. Introduction

Incremental analog-to-digital converters (IDCs) are popular for many of today's instrumentation and process control applications that need to convert the analog output of a sensor for processing or storage purposes [1], [2]. To increase the input dynamic range and to obtain the maximum noise and common-mode rejection, most IDCs adopt the fully differential input structures instead of the single-ended or pseudo-differential ones [3], as shown in Fig. 1.

A typical 1st-order fully differential incremental $\Delta\Sigma$ modulator is shown Fig. 2. For a normalized $V_{\text{in}} \in [-1, 1]$, the feedback must be bipolar ($\pm 1$) as well for signal balancing [1]. Conventionally, this fully differential modulator is analyzed in a similar way as its single-ended counterpart without considering their different feedback characteristics [4]. This may cause flaws in the actual design. Firstly, without special control schemes, the feedback signal range is 2 in a fully differential modulator, less information can be encoded in each quantization cycle [5]. It then requires more cycles to achieve the same quantization noise as that of a single-ended topology. Therefore, the modulator's efficiency is degraded amid an improved input common-mode rejection. Moreover, it is often mentioned in the literature (and is true) that the IDC needs to be reset before each conversion [1], while detailed analysis has not been performed on the modulator dynamics right after this reset operation, especially for the fully differential topology.

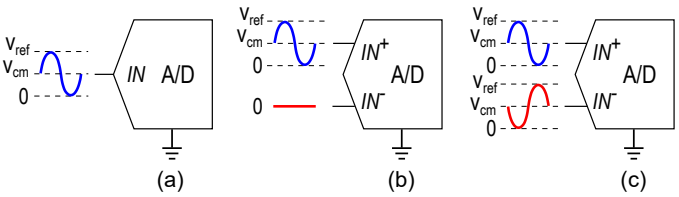


Fig. 1. Typical unipolar A/D input structures: (a) single-ended input; (b) pseudo-differential input; (c) fully differential input.

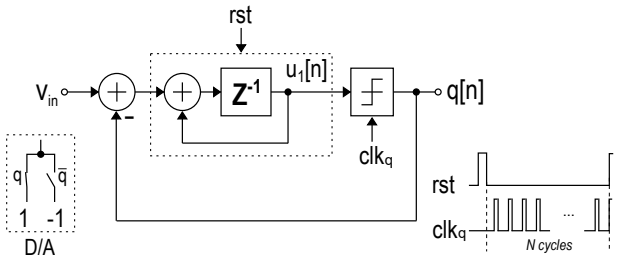


Fig. 2. Model of a 1st-order fully differential incremental $\Delta\Sigma$ modulator using 1-bit quantizer and delaying integrator, with its simplified timing diagram and a typical feedback implementation.

In this paper, the time-domain operation of a fully differential incremental modulator (1st- and 2nd-order) is revisited. Particularly, the influence of bipolar feedback on the quantization noise of the modulator is analyzed. Based on the analysis, an initial feedback zeroing control scheme is introduced to improve the modulator performance. Moreover, the maximum number of codeword that can be produced by an ideal modulator is mathematically derived. Guided by the derivation, a control scheme is proposed to achieve 1.5-bit effective feedback without changing the D/A design. Using the proposed initial feedback zeroing and 1.5-bit feedback control, the theoretically minimum quantization noise of a fully differential modulator can be achieved. To implement the control schemes, only minor modifications on the conventional IDC's digital controller are required.

## II. First-order Fully Differential Modulator

In the rest of this paper, signals are all normalized against the IDC's reference signal and the modulator output is decoded with an ideal filter.

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### A. Operation of The Modulator

As shown in Fig. 2, the modulator works in its transient mode and is reset before each conversion. It then operates for $N$ quantization cycles ($clk_{\rm q}$) to generate a digital bitstream $q$, which can be used to estimate the actual input $v_{\rm in}$ using a digital filter. For IDCs, $N$ is defined as the oversampling ratio (OSR). The quantizer in Fig. 2 is defined as

$$q[n] = \begin{cases} 1 & u_1[n] \geqslant 0, \\ -1 & u_1[n] < 0, \quad n \geqslant 1. \end{cases} \tag{1}$$

After reset, the initial integrator output $u_1[0]$ is 0. At the $n^{\rm th}$ quantization cycle, $u_1[n]$ satisfies a discrete-time difference equation of

$$u_1[n] = u_1[n-1] + v_{\rm in} - q[n-1], \quad n \geqslant 1. \tag{2}$$

By simplifying the recursive relationship (2),

$$u_1[n] = n \cdot v_{\rm in} - \sum_{i=0}^{n-1} q[i] \triangleq n \cdot v_{\rm in} - s_{\rm n}, \quad n \geqslant 1, \tag{3}$$

where $s_{\rm n}$ is the running sum of $q[0{:}n{-}1]$. Refer to (1), the quantizer is comparing $u_1[n]$ with 0 and the digital output of the modulator is

$$q[n] = \begin{cases} 1 & v_{\rm in} \geqslant s_{\rm n}/n, \\ -1 & v_{\rm in} < s_{\rm n}/n, \quad n \geqslant 1. \end{cases} \tag{4}$$

One can derive the modulator's digital output sequence following (3)(4) for any input signal.

### B. Initial Feedback Zeroing

For single-ended IDC with unipolar feedback, $q[0]$ is 0 after reset. However, for fully differential IDC, the effective quantizer output $q[0]$ is $-1$ after reset in typical feedback implementations (see Fig. 2 or [6], [7]). Without special timing control, a feedback signal of $+1$ will be integrated in the first cycle, along with $v_{\rm in}$. This seems to be trivial as the modulator loop can react correspondingly to achieve signal balancing over time and ensure $u_1[n]{\in}[-1, 1]$. That is why almost no fully differential IDC designs have taken this initial non-zero feedback seriously. Indeed, it will greatly affect the modulator dynamics and degrade the modulator performance as analyzed below.

For an OSR of $N$, $\{n \in \mathbb{Z}^+,\ 1 \leqslant n \leqslant N\}$ holds in (3) and (4). Meanwhile,

$$s_{\rm n+1} = \begin{cases} s_{\rm n} + 1 & q[n] = \ \ 1, \\ s_{\rm n} - 1 & q[n] = -1, \quad n \geqslant 1. \end{cases} \tag{5}$$

Refer to (4), the modulator is essentially comparing $v_{\rm in}$ to a series of thresholds $s_{\rm n}/n$ to generate the digital outputs. For example, if $v_{\rm in} = 1/4$ and $s_1 = q[0] = -1$, in the first quantization cycle, $(1/4) > (-1/1)$, therefore $q[1] = 1$. In the second cycle, $(1/4) > (0/2)$, $q[2] = 1$. In the third cycle, $(1/4) < (1/3)$, $q[3] = -1$, and so on and so forth to produce an $N$-bit bitstream. For a certain range of inputs, the same output sequence will be generated. This sequence is called a codeword (the more the better), the corresponding input range is its code length [8], and the start and end value of this input range are called code transition points. These transition points are all expressed in the form of $s_{\rm n}/n$, where

$$s_{\rm n} = \sum_{i=0}^{n-1} q[i] \in \mathbb{Z}, \quad \text{and} \tag{6}$$

$$q[0] - (n-1) \leqslant s_{\rm n} \leqslant q[0] + (n-1). \tag{7}$$

Theoretically, $2{\times}(n{-}1)$ more new $s_{\rm n}/n$ values or transition points will be introduced at the $n^{\rm th}$ quantization cycle according to (7). However, as $s_{\rm n}$ and $n$ are not always mutually prime and repeated $s_{\rm n}/n$ values could occur, less new transition points result. As an example, Table I lists all the possible values of $s_{\rm n}$ in each quantization cycle with $N = 8$ and $s_1{=}q[0]{=}{-}1$. When $n = 6$, only two new transition points ($\pm 4/6$) are introduced. To derive more codeword, the number of common divisors between $s_{\rm n}$ and $n$ must be minimized. Since the parity of $s_{\rm n}$ at the $n^{\rm th}$ cycle depends on $q[0]$ (see (7) or Table I), by blocking (or zeroing) the feedback signal during the first integration cycle, namely $q[0] = 0$, $s_{\rm n}$ will be odd when $n$ is even, and vice versa (see Table I). In this way, the total number of codeword can be increased.

The simulated transfer curve of a fully differential 1st-order incremental $\Delta\Sigma$ modulator with $q[0] = -1$ and $q[0] = 0$ is shown in Fig. 3. It can be observed that finer quantization steps and more codewords result when the initial feedback is zeroed. It also halves the dead-zone of the modulator. For different OSR, the total number of codeword and output mean squared

TABLE I
ALL POSSIBLE VALUE OF $s_{\rm N}$ IN EACH QUANTIZATION CYCLE WITH $N = 8$, FOLLOWING EQ. (5).

| $n$ | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| $s_{\rm n}$ | $-1^{\dagger}_{(0)}$ | $-2_{(-1)}$ | $-3_{(-2)}$ | $-4_{(-3)}$ | $-5_{(-4)}$ | $-6_{(-5)}$ | $-7_{(-6)}$ | $-8_{(-7)}$ |
| | | $0_{(1)}$ | $-1_{(0)}$ | $-2_{(-1)}$ | $-3_{(-2)}$ | $-4_{(-3)}$ | $-5_{(-4)}$ | $-6_{(-5)}$ |
| | | | $1_{(2)}$ | $0_{(1)}$ | $-1_{(0)}$ | $-2_{(-1)}$ | $-3_{(-2)}$ | $-4_{(-3)}$ |
| | | | | $2_{(3)}$ | $1_{(2)}$ | $0_{(1)}$ | $-1_{(0)}$ | $-2_{(-1)}$ |
| | | | | | $3_{(4)}$ | $2_{(3)}$ | $1_{(2)}$ | $0_{(1)}$ |
| | | | | | | $4_{(5)}$ | $3_{(4)}$ | $2_{(3)}$ |
| | | | | | | | $5_{(6)}$ | $4_{(5)}$ |
| | | | | | | | | $6_{(7)}$ |

†: The footnote numbers are $s_{\rm n}$ with $q[0] = 0$ (with zero initial feedback).

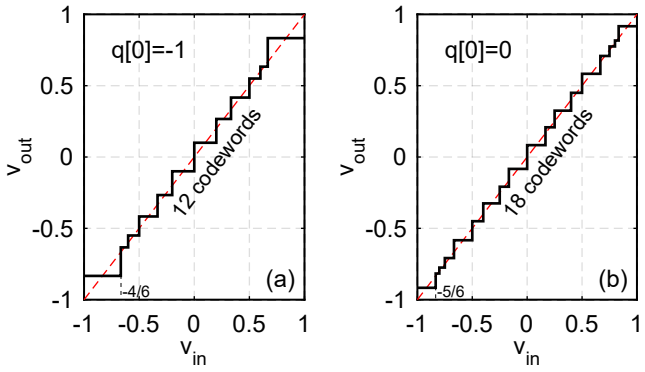


Fig. 3. Transfer curve of a 1st-order fully differential incremental $\Delta\Sigma$ modulator with (a) $q[0] = -1$ and (b) $q[0] = 0$, with $N = 6$.

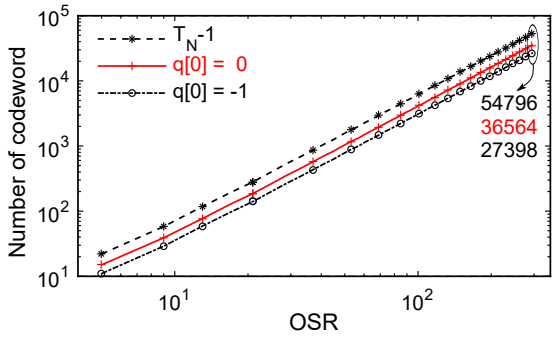


Fig. 4. The total number of codeword of the 1st-order fully differential modulator with different initial feedback and OSR.

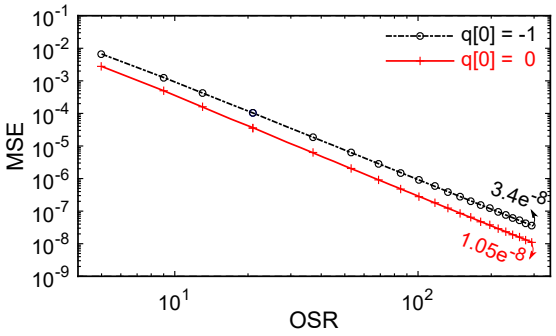


Fig. 5. Output MSE of the 1st-order fully differential modulator with different initial feedback and OSR.

error (MSE) are shown in Fig. 4 and Fig. 5, respectively. Here the output MSE is calculated via [9]

$$MSE = E[(v_{\text{in}} - \hat{v}_{\text{in}})^2] = \sum_{i=1}^{N_{\text{code}}} \left(\frac{\Delta_{\text{i}}}{2} \cdot \frac{\Delta_{\text{i}}^2}{12}\right), \tag{8}$$

where $N_{\text{code}}$ is the total number of the output codeword, $\Delta_{\text{i}}$ is the code length of the $i^{\text{th}}$ codeword. Though seems trivial, the initial feedback signal greatly affects the modulator dynamics and 3.4× lower quantization noise can be obtained by zeroing this feedback.

### C. Inherent 1.5-bit Feedback

Based on the above analysis, at the $n^{\text{th}}$ quantization cycle, only if $s_{\text{n}}$ and $n$ are mutually prime, new $s_{\text{n}}/n$ values can be generated. Therefore, the total number transition points can be derived with the help of the Euler's totient function $\varphi(n)$ [10]. Firstly, the quantization cycle $n$ can be expressed with

$$n = p_1^{k_1} \cdot p_2^{k_2} \cdot p_3^{k_3} \cdots p_{\text{r}}^{k_{\text{r}}}, \tag{9}$$

where $p_1 \sim p_{\text{r}}$ are prime numbers, and $k_1 \sim k_{\text{r}} \in \mathbb{Z}^+$ are their exponents, respectively. Then, $\varphi(n)$ is

$$\varphi(n) = \prod_{i=1}^{r} p_{\text{i}}^{k_{\text{i}}-1}(p_{\text{i}} - 1). \tag{10}$$

Because $s_{\text{n}}$ is bipolar and considering the three extra transition points ($\pm 1$, 0), the total number of transition points $T_{\text{N}}$ for an OSR of $N$ is

$$T_{\text{N}} = 2\sum_{n=2}^{N} \varphi(n) + 3. \tag{11}$$

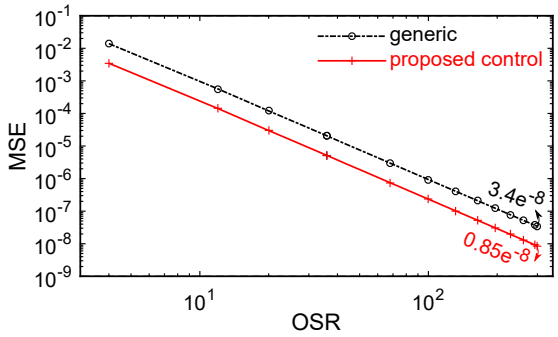


Fig. 6. Output MSE of the 1st-order fully differential modulator: generic topology and with the proposed initial feedback zeroing and 1.5-bit feedback.

This value is a rigorous theoretical calculation instead of an estimation as in [8]. For example, for an OSR of 300, the maximum number of codeword that can be generated by a 1st-order fully-differential modulator is $T_{300} - 1 = 54796$. However, as shown in Fig. 4, even with initial feedback zeroing, the number of output codeword is still far less than this value. The reason is that compared with a single-ended topology, not all the transition points can be hit in a fully differential design due to its wide feedback range. Specifically, when $n$ is odd, all the transition points with $s_{\text{n}}$ being odd are not generated (see Table I with $q[0] = 0$).

To retrieve all these transition points and fully utilize the modulator, different feedback signals can be applied to the modulator based on the status of $s_{\text{n}}$ and the integrator output $u_1[n]$. Herein, a 1.5-bit inherent feedback is proposed with

$$\text{feedback} = \begin{cases} 1 & u_1[n] \geqslant 0 \quad \text{and} \quad s_{\text{n}} \geqslant 0; \\ 0 & u_1[n] \geqslant 0 \quad \text{and} \quad s_{\text{n}} < 0, \\ & \text{or } u_1[n] < 0 \quad \text{and} \quad s_{\text{n}} > 0; \\ -1 & u_1[n] < 0 \quad \text{and} \quad s_{\text{n}} \leqslant 0. \end{cases} \tag{12}$$

This feedback scheme can be achieved with minor modifications from the conventional 1-bit D/A topology by adding an accumulator to calculate $s_{\text{n}}$. This accumulator can be shared by the digital filter (e.g., CIC filter [1]) for resource savings. Using the initial feedback zeroing and the 1.5-bit feedback scheme, all the possible transition points $T_{\text{N}}$ shown in Fig. 4 can be hit thus the best modulator performance (encoding efficiency) can be achieved. Fig. 6 shows the simulated MSEs of the modulator for different OSRs. Compared with the generic topology, 4× lower quantization noise results. Fig. 7 shows an exemplary feedback control implementation using standard logic gates. Worthy to mention that other implementations that can achieve zeroed initial feedback and satisfy (12) will also work.

### D. Digital Filtering

To convert the high data-rate digital bitstream $q$ to the desired multi-bit output, a digital filter and OSR-to-1 decimator are required [11]. After the above control modifications, classical filters, such as the *sinc* and cascade-of-integrator filters, still apply as the modulator follows the signal balancing property [12].

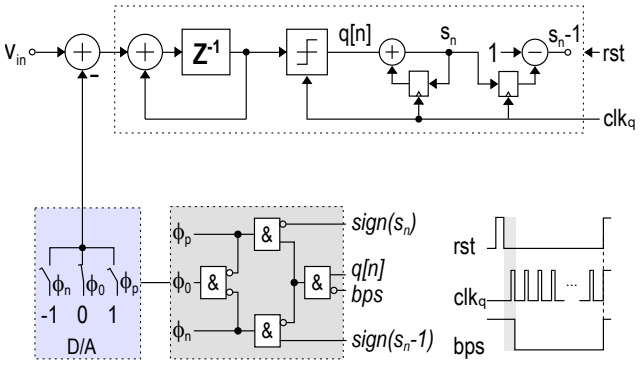


Fig. 7. Exemplary implementation of the initial feedback zeroing and 1.5-bit feedback control ($s_n$ is a signed number).

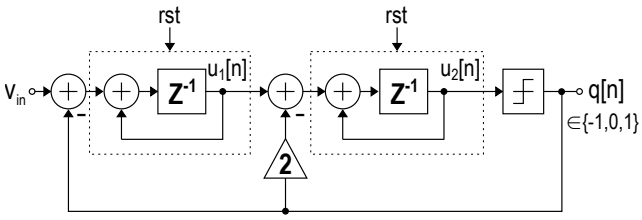


Fig. 8. A typical model of a 2nd-order incremental $\Delta\Sigma$ modulator.

## III. For Higher-order Fully Differential Incremental Modulator

Without loss of generality, a typical 2nd-order fully differential incremental modulator shown in Fig. 8 is used to verify the MSE improvement in higher-order modulators using the initial feedback zeroing and 1.5-bit feedback scheme. The time-domain integrator outputs $u_1[n]$ and $u_2[n]$ can be derived following the steps introduced in Section II-A, with

$$u_2[n] = \frac{n(n-1)}{2} \cdot v_{\text{in}} - \sum_{i=0}^{n-1}(n+1-i)q[i] \triangleq r_{\text{n}} \cdot v_{\text{in}} - s_{\text{n}}, \quad n \geqslant 1. \tag{13}$$

Different from that of the 1st-order modulator, there are two clock delays before the actual input $v_{\text{in}}$ appears in $u_2[n]$. Therefore, the feedback signal $q[0]$, $q[1]$ must be all zeroed. This will result an integrator output $u_1[2] = 2v_{\text{in}}$. To avoid overflow, appropriate signal scaling can be used in real implementations.

Following Section II-C, the maximum number of transition points for this 2nd-order modulator can also be derived by analyzing the possible values of $r_{\text{n}}$ and $s_{\text{n}}$ in (13). Because of their second-order dependencies on $n$, the number of transition points in this case increases rapidly with $n$ but are highly irregular. As a result, it is mathematically complicated to tick out the repeated $s_{\text{n}}/r_{\text{n}}$ values and calculate the precise number of transition points $T_{\text{N}}$. Herein an upper bound of $T_{\text{N}}$ is derived using the possible values of $s_{\text{n}}$ in each quantization cycle, with

$$T_{\text{N}} \leqslant \sum_{n=2}^{N}(n-1)(n-2)+3, \quad N \geqslant 2. \tag{14}$$

Fig. 9 and Fig. 10 are the simulated codeword and MSE of this 2nd-order incremental modulator, respectively. The resulted

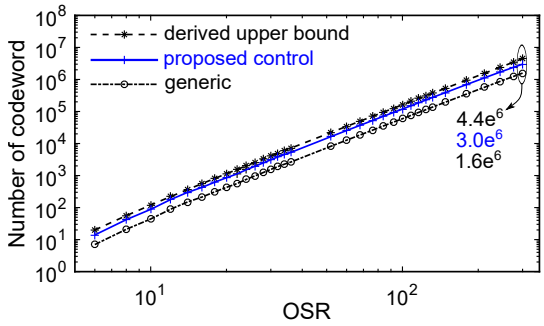


Fig. 9. The total number of codeword of the 2nd-order fully differential modulator with different OSR.

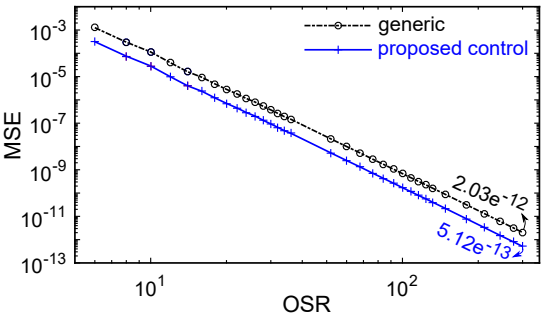


Fig. 10. Output MSE of the 2nd-order fully differential modulator (input dead-bands are excluded in the MSE calculation).

MSE is also reduced by 4× compared to its generic topology thanks to the increased number of codeword.

Worthy to mention that only 1-bit quantizer and delaying integrators are analyzed in this paper. However, the analysis presented applies to other modulator typology using a multi-bit quantizer and/or non-delaying integrator as well. Moreover, the purpose of all the other popular techniques like higher-order modulators, MASH topology, residue counting, exponential integration, etc. were all proposed with the aim of increasing the number of codeword generated by the modulator. Techniques proposed in this paper achieves the goal via basic control modifications.

## IV. Conclusion

In this paper, a control scheme for the fully differential incremental modulator is proposed after a detailed time-domain analysis. It is found that the initial status of the feedback would greatly affect the modulator dynamics but was overlooked by most of the IDC designs. By adopting an initial feedback zeroing (blocking) scheme, more codewords can be generated by the modulator thus lower quantization noise results without increasing the conversion cycles. Moreover, the maximum number of codeword that can be generated by the modulator is mathematically derived. Following this derivation, a 1.5-bit effective feedback scheme is proposed by using the 1-bit quantizer. Using the proposed control scheme, the quantization noise of the modulators that are analyzed in this paper can be decreased by 4× than their generic typology, which is theoretically the lowest quantization noise can be achieved. The proposed control is very straightforward in terms of silicon implementation as well.

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