Incremental Delta-Sigma ADC with Reduced Conversion Cycles via Quantization-Skip

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2025 IEEE International Symposium on Circuits and Systems (ISCAS) | 979-8-3503-5683-0/25/$31.00 ©2025 IEEE | DOI: 10.1109/ISCAS56072.2025.11044181

***Abstract*—This paper presents a technique to effectively reduce the number of conversion cycles of the 1st-order incremental delta-sigma data converter (IADC1). Typically, an IADC1 requires 2^N cycles to achieve N-bit resolution if using a sinc[1] filter for reconstruction. The proposed quantization-skip technique can effectively reduce the average conversion cycles and, therefore, the energy consumption of an IADC1. Specifically, during conversion, the quantizer output is predicted using the previous bitstream pattern to achieve automatic bitstream fill-in without analog domain operations. Behavioral level simulations show that this technique can reduce the conversion cycles by 24% on average (maximum reduction of ∼50%) with little digital overhead.**

***Index Terms*—Incremental delta-sigma ADC, quantization-skip, bitstream fill-in, IADC.**

I. Introduction

Incremental delta-sigma ($\Delta\Sigma$) analog-to-digital data converter (IADC) is often the prioritized option for high-resolution sensor interfaces [1], [2], as it can perform sample-by-sample conversion and allows easy multiplexing between multiple input channels [3], [4]. Unlike its free-running $\Delta\Sigma$ counterpart, IADCs are not subject to idle tones and require only simple reconstruction filters for output reconstruction [5], [6]. Although plenty of IADC architectures have been proposed, the generic 1st-order IADC (IADC1 as in Fig.1) consisting of a modulator followed by a digital filter is still popular in many scenarios such as hybrid data converters including extended-counting, coulomb counter in the battery management system, etc., given its simplicity, robustness, and uniform reconstruction filter weights [7], [8].

The main limitation of an IADC1 is its large conversion cycles (i.e., oversampling ratio, OSR), with 2^N cycles required to achieve N-bit resolution when using a counter for digital reconstruction [9]. Its OSR can be reduced using higher-order digital filters, such as a two-stage cascaded-of-integrators filter, while it introduces quantization error spikes and mandates costly quantizer dithering [5]. Another method to reduce its OSR is using a hybrid architecture that combines IADC1 with other ADC architectures, such as successive-approximation ADC, to achieve the target resolution [10], [11]. IADC1 can also be used in multi-stage noise-shaping (MASH) or extended counting architectures to achieve high-resolution conversion at a low OSR [12].

This paper presents a quantization-skip technique to reduce the number of conversion cycles of an IADC1 while maintaining its quantization noise level. The core idea of this technique is to utilize the existing quantizer output pattern, namely, bitstream, to effectively predict the subsequent modulator output bit (or a few bits). An example implementation of this quantization-skip technique can reduce the IADC1's conversion cycle by about 24% on average.

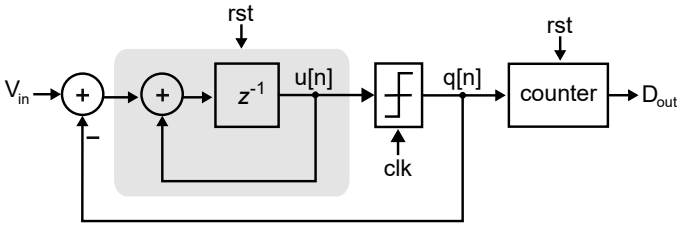


Fig. 1: Generic model of a first-order incremental $\Delta\Sigma$ ADC using a delaying integrator and a counter for output reconstruction.

The rest of this paper is organized as follows. Section II revisits the IADC1 operation to pave the way for introducing the digital-assisted quantization-skip technique. Section III presents the operation principle, behavioral model, and implementation of the proposed scheme, followed by a conclusion in Section IV. Although this paper utilizes a 1-bit quantizer to illustrate the quantization-skip technique, the analysis also applies to IADC1 using a multi-bit quantizer.

II. Incremental $\Delta\Sigma$ Modulator Revisit

A. Basic Operation

Fig. 1 shows a genetic model of an IADC1 consisting of a delayed integrator, a 1-bit quantizer, and a digital filter (a counter). For simplicity of analysis (does not affect the conclusion), assuming V_{in} is constant during each conversion and all signals are normalized to the system reference V_{ref} [13]. As the integrator output $u[n]$ will be reset before each conversion, $u[0] = 0$ holds. $q[n] \in [-1, 1]$ is the quantizer output with $q[0] = 0$. At the n^{th} quantization cycle, $u[n]$ can be expressed as

$$u[n] = u[n-1] + V_{\text{in}} - q[n-1], \quad n \geqslant 1. \tag{1}$$

with

$$q[n] = \begin{cases} 1 & u[n] \geqslant 0, \\ -1 & u[n] < 0, \quad n \geqslant 1. \end{cases} \tag{2}$$

By using (1) and (2),

$$u[n] = n \cdot V_{\text{in}} - \sum_{i=0}^{n-1} q[i], \quad n \geqslant 1. \tag{3}$$

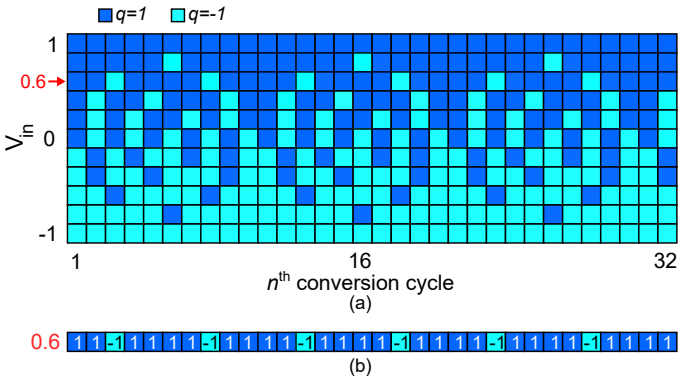


Fig. 2: (a) A raw bitstream color map of an IADC1 at different cycles and different inputs to illustrate the repeated occurring bit patterns; (b) $q[n]$ pattern at an input of 0.6 as an example.

During conversion, $u[n]$ must be bounded within the quantizer input range, namely

$$-1 \leqslant u[n] \leqslant 1. \tag{4}$$

Therefore, the estimated V_{in} from the modulator digital output would be bounded by

$$\frac{-1}{n} + \frac{1}{n}\sum_{i=0}^{n-1} q[i] \leqslant \widehat{V}_{\text{in}} \leqslant \frac{1}{n} + \frac{1}{n}\sum_{i=0}^{n-1} q[i]. \tag{5}$$

For an OSR of N, the estimated input is $1/N \cdot \sum_{i=1}^{N-1} q[i]$, and the modulator quantization error is bounded by $\pm 1/N$.

B. A Closer Look at the Bitstream

To investigate the inherent bitstream property of the modulator, using OSR=32 as an example, Fig. 2 shows $q[n]$ at different quantization cycles n for different V_{in}. It can be observed that there are repeated patterns in $q[n]$ for a given V_{in}, such as the "-1,1,1,1,1" repeat pattern at an input of 0.6 [Fig. 2(b)], which is effectively an undesired idle tone in free-running $\Delta\Sigma$ ADC. However, such a pattern can be utilized to perform automatic bitstream fill-in by skipping some quantization cycles. In the above example, the cycle that produces "-1" can be skipped (auto-fill-in) whenever four consecutive "1s" appear. In the following, we aim to find a pattern that can be used for bitstream auto-fill-in and achieve maximum average conversion cycle savings under different V_{in}.

III. Proposed Quantization-Skip Technique

A. Operation Principle

Considering the trade-off between digital control overhead and the number of conversion cycles saved, we first investigated the bitstream pattern consisting of 4-bit. As a result, two bitstream patterns can be utilized to achieve $q[n]$ auto-fill-in: "-1,-1,1,-1" and "1,1,-1,1". For example, for an input $V_{\text{in}} = 0.5$ under an OSR of 1024, the modulator bitstream repeats the "1,1,-1,1" pattern by ∼255 times. That is to say, if the quantizer output was "1,1,-1", the next output is a definite "1" without analog-domain operations (also valid after involving circuit noise and non-idealities, as discussed later). Using OSR=1024 as an example, Fig. 3(a) presents the pattern occurrences at different V_{in}. Using the above two patterns for auto-fill-in, the IADC1's conversion cycle can be saved by ∼17% on average.

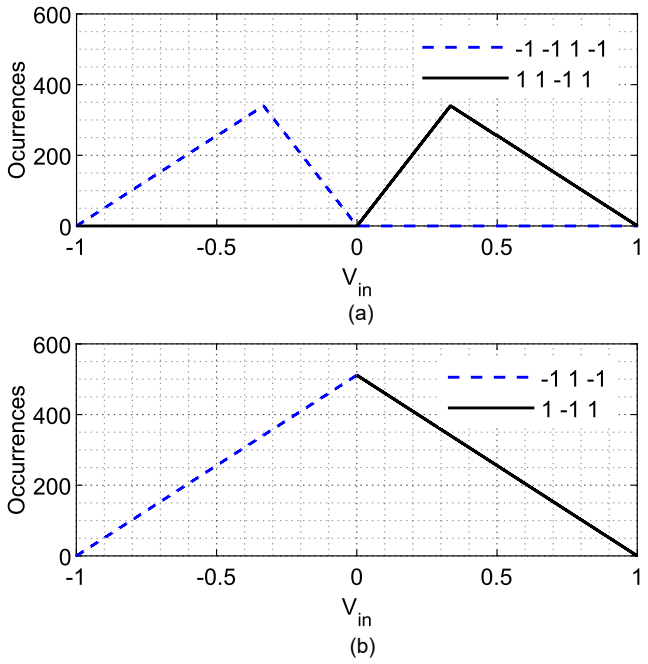


Fig. 3: With an OSR of 1024, (a) the occurrence of a predefined 4-bit bitstream pattern, and (b) the occurrence of a predefined 3-bit bitstream pattern at different V_{in}.

For a fully differential IADC1, the input polarity can be handily known (e.g., using the first few bits to estimate), and a 3-bit bitstream pattern can be used to achieve quantization-skip for even better performance. The pattern applied to negative inputs is "-1,1,-1" (i.e., a definite "-1" if a "-1,1" pattern appears), while the "1,-1,1" bitstream pattern applies to positive inputs, as shown in Fig. 3(b). As a result, about 24% of IADC1's conversion cycles can be saved on average (maximum ∼50% for input with small amplitude).

B. Behavioral Model and Influence of Circuit Non-Idealities

A behavioral model is built to validate the above scheme under practical design conditions such as comparator offset and circuit noise (Gaussian noise used in the model). By adding a comparator offset of 5 m (normalized to V_{ref}) and an input-referred thermal noise voltage of -68 dBFS (i.e., 400 μ) to the model (values selected based on typical process data and practical design needs), the results of Fig. 3(b) changed for inputs around 0, a region more susceptible to non-idealities, and the above-mentioned "-1,1,-1" and "1,-1,1" bitstream pattern does not appear repetitively. However, by employing the quantization-skip technique, that is, forcing a "-1" after "-1,1" for any negative V_{in} and a "1" after "1,-1" for any positive V_{in}, IADC1 still operates correctly. Fig. 4 shows the quantization error for a 10-bit IADC1 for V_{in} around 0, which is well-bounded within ± 0.5 LSB.

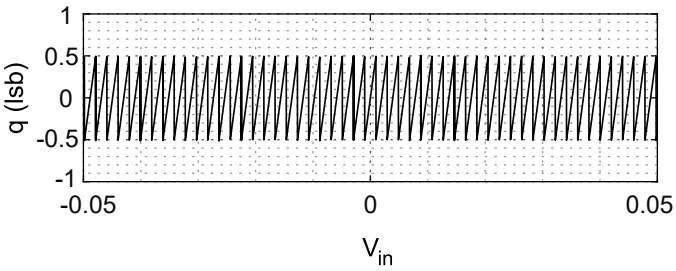


Fig. 4: Quantization error for small V_{in} after applying quantization-skip (with an effective OSR being 1024).

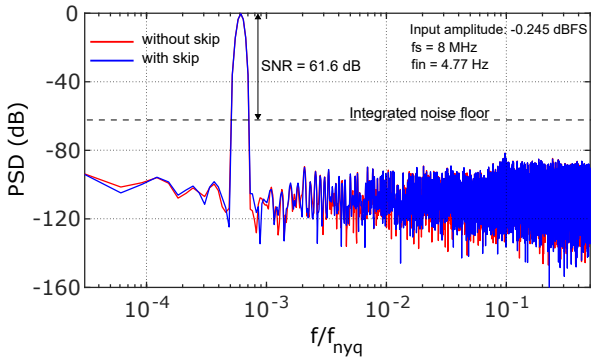


Fig. 5: Modulator output PSD for a -0.245 dBFS (with -68 dBFS input gaussian noise), 4.77 Hz input with OSR=1024 as an example (with and without using quantization-skip, behavioral simulation).

Fig. 5 shows the modulator output power spectral density (PSD) for a noisy input of -0.245 dBFS at about 5 Hz (this technique applies mainly for low-frequency signals) with and without applying the above-stated quantization-skip, where OSR = 1024 is used as an example. With quantization-skip, a signal-to-noise ratio (SNR) of 61.6 dB is achieved, corresponding to 10-bit resolution as expected. In practical operation, the quantization-skip would effectively result in a non-uniform input sampling (i.e., more cycles are skipped for small amplitude inputs as in Fig. 3(b), thus faster conversion). To present the PSD, we performed a uniform sampling (i.e., 1024 cycles per conversion; the modulator enters an idle state if it finishes one conversion using less than 1024 cycles).

In addition, quantization skip can assist in suppressing circuit noise, including the sampling noise and noise introduced by the amplifier, as they are integrated for fewer cycles. This is another advantage of the proposed technique.

C. Implementation of an IADC1 with Quantization-Skip

For an IADC1 using quantization-skip (bitstream auto-fill-in), it is necessary to integrate an input of $2 \cdot V_{\text{in}}$, and also the corresponding feedback in the successive cycle to maintain correct signal levels in the modulator. Therefore, after every skipping, (1) is modified to perform the summation of $2 \cdot V_{\text{in}}$, $q[n-1]$, and $q[n-2]$. For the bit pattern we selected (i.e., skip one after "-1,1" or "1,-1"), $q[n-1] + q[n-2] = 0$. This means that the feedback signal is null. The feedback capacitors, typically the same size as the sampling capacitors,

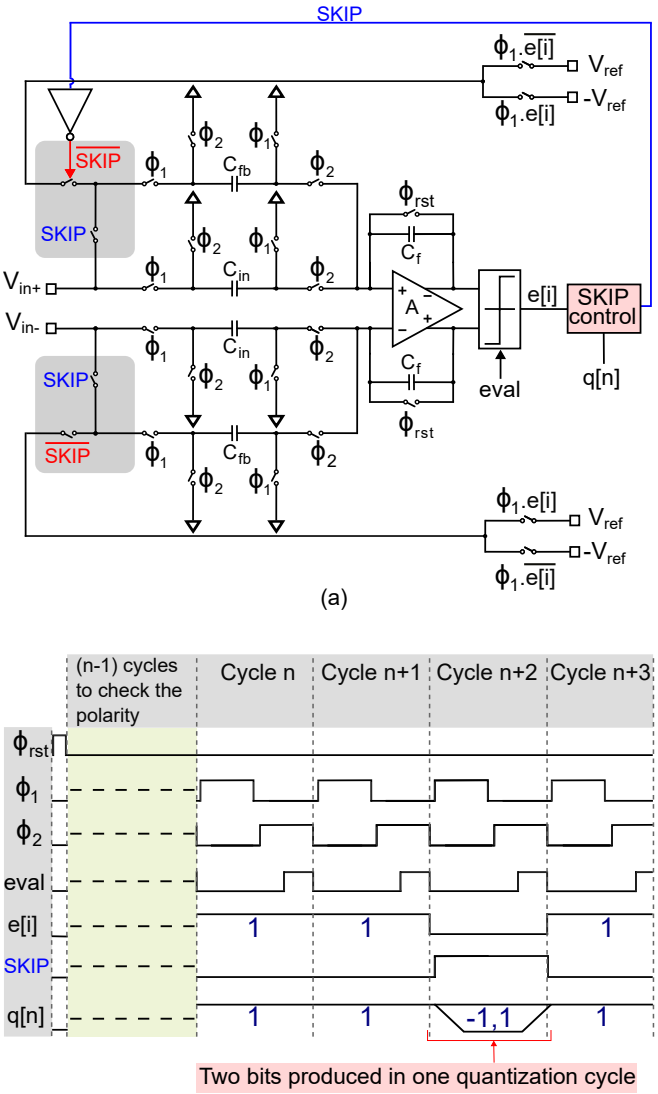


Fig. 6: (a) Example implementation of an IADC1 with quantization-skip; (b) waveforms of a few critical signals showing its operation.

can be used to sample the input together and achieve the $2 \cdot V_{\text{in}}$ integration without extra hardware overhead.

An example implementation is shown in Fig. 6(a). Once the predefined pattern appears (i.e., a "-1,1" or a "1,-1"), a *SKIP* signal is triggered to double the input sampling capacitance. The generation of *SKIP* involves simple digital flip-flops with negligible power overhead. Meanwhile, no amplifier reconfiguration is required since the error amplifier in the integrator drives the same load. Fig. 6(b) shows the waveforms of a few critical signals, with a positive input voltage as an example to show how the quantization-skip technique works. For example, two output bits are produced simultaneously in the cycle n+2 without analog-domain operations. An integrator gain of 0.4 is applied to avoid saturating the integrator when integrating $2 \cdot V_{\text{in}}$. Fig.7 shows the output distribution of $u[n]$ of the IADC1 model, which can be well-bounded within ± 1. Fig. 8 shows

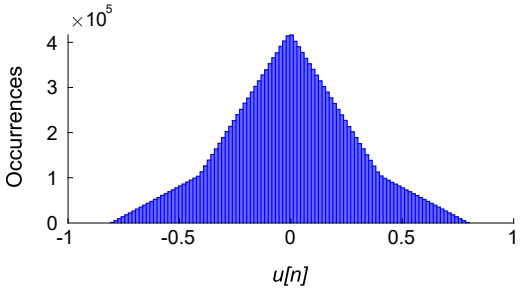
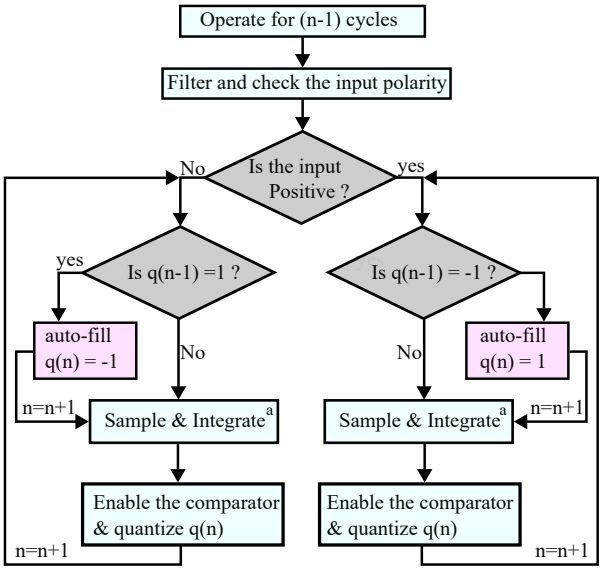


Fig. 7: Integrator output $u[n]$ distribution (from model).



a: Sample and integrate of $2.V_{in}$ after auto-filling.

Fig. 8: Operation of the skip control: q(n) represents the quantizer output at the n^{th} cycle. The loop stops when n reaches the required OSR.

the flow chart of the algorithm used for the quantization-skip technique, where the first few cycles are used to determine the input polarity. The scheme still works for erroneous polarity determination for very small V_{in}. Fig. 9 shows the simulated PSD for a $\sim$5 Hz input at -0.245 dBFS, with SNR = 50.53 dB for an OSR of 256 (a smaller OSR and a lower f_s used considering the simulation time).

IV. Conclusion

In this paper, we proposed a technique to reduce the number of conversion cycles using a quantization-skip technique for IADC1 by about 24% on average for low-frequency signals. This technique can also reduce the integrated thermal noise by the same amount. This paper presented its operation principle, behavioral modeling, and example schematic implementation. It can be handily employed in incremental ADC architectures such as extended-counting, multistep conversion, etc.

Acknowledgment

This publication was made possible by NPRP grant NPRP13S-0122-200135 from the Qatar National Research Fund (a member of Qatar Foundation). The statements made herein are solely the responsibility of the authors.

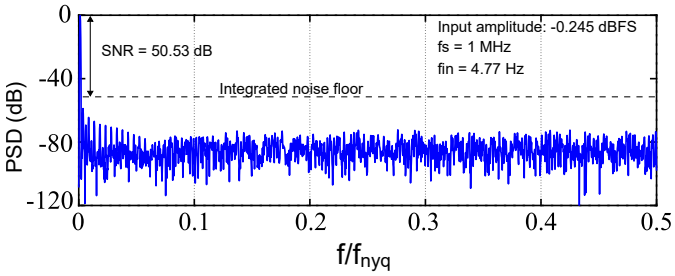


Fig. 9: Simulated modulator output PSD with quantization-skip using OSR = 256, schematic simulation.

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