Analysis of Output Ripple Shape and Amplitude in Chopper Instrumentation Amplifier

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***Abstract*—In this brief, we analyzed the output ripple in a capacitively-coupled chopper-based instrumentation amplifier (CCIA). Our analysis found that the shape and amplitude of the output ripple of the CCIA are determined by five design parameters, namely amplifier offset, transconductance, chopping frequency, Miller compensation capacitance, and the nulling resistor. With different design specifications, the CCIA ripple appears in four different shapes, including triangular ripple, RC-settling ripple, square ripple, and step-change ripple. These findings are verified by the silicon results. As the cause of each ripple shape varies, this analysis serves as a guideline for designing practical chopper-based amplifiers and their corresponding ripple reduction techniques.**

***Index Terms*—Capacitively-coupled chopper-based instrumentation amplifier, CCIA, chopper, instrumentation amplifier, ripple formation, ripple shape, ripple reduction.**

I. Introduction

SIGNAL acquisition for sensing applications requires a high-performance amplifier. The main requirements for the amplifier to preserve the input signal quality are low noise, precise gain, and high common-mode rejection ratio (CMRR) [1]. Instrumentation amplifiers (IAs) are frequently used in sensor readout circuits to address these challenges. However, imperfections in amplifiers induce errors in the system, which introduces an output voltage even with zero input. This voltage can be referred to input and treated as a DC offset. Typically, the offset voltage is of tens to hundreds of micro-volts in bipolar technology, but it is much higher in CMOS technology (mill-volts level) [2]. IAs with high gain can be saturated merely by the offset voltage if it is overlooked. Various techniques have been employed to minimize device/system offset, such as careful layout matching, the use of large transistors, and post-trimming. Although these one-time offset reduction techniques are easy to implement, they cannot handle offset drifts. Therefore, dynamic offset reduction techniques, such as auto-zeroing, correlated double sampling, and chopper stabilization, are more favorable in IA designs [3].

Chopper stabilization techniques are used in chopper-based IAs to suppress the low-frequency disturbances ($1/f$ noise and DC offset). However, chopping cannot remove low-frequency noise and offset but only modulates the disturbances to a higher frequency. Consequently, the disturbances will appear as an AC component (ripple). This offset-induced ripple could reduce the usable output swing [4], especially in deep submicron processes that have limited voltage headroom for the outputs. Thus, the removal or suppression of the IA output ripple is critical to providing sufficient swing.

In order to achieve a small gain error and stable operation under different conditions, a two-stage amplifier with Miller compensation is used as the IA core [5], [6], as shown in Fig. 1. The output ripple of the IA is estimated to be a triangular-shaped signal. The amplitude is derived using the offset value, transconductance, chopping frequency, and Miller compensation capacitance of the core amplifier [1]. However, this estimation is not always true and may cause design flaws if a ripple suppression scheme is developed based on this estimation without considering the actual design parameters.

To the best of the authors' knowledge, there is no existing literature analyzing the formation of the IA output ripple under different design conditions. This brief presents a thorough analysis of ripple formation for a capacitively-coupled chopper-based instrumentation amplifier (CCIA), including the ripple shape and amplitude. The remainder of this brief is organized as follows. Section II presents the modeling of the formation and shapes of ripples, which are classified into four categories. Additional design parameters to be taken into consideration are discussed as well. Section III presents the silicon results to validate the analysis. Section IV discusses the impact of the findings on existing ripple reduction techniques. Section V concludes the brief.

II. Modeling of CCIA Output Ripple Shape and Amplitude

The schematic of a typical CCIA is shown in Fig. 1. The core of this IA is a two-stage amplifier with Miller compensation. Choppers are inserted in the signal path and feedback path to modulate the signals between DC and the chopping frequency. Circuit imperfections are referred to the input of the two-stage amplifier as an offset voltage V_{os}. To examine this offset-induced output ripple, input of the second stage is assumed to be virtual ground, input signals ($v_{\text{in}+/-}$) are

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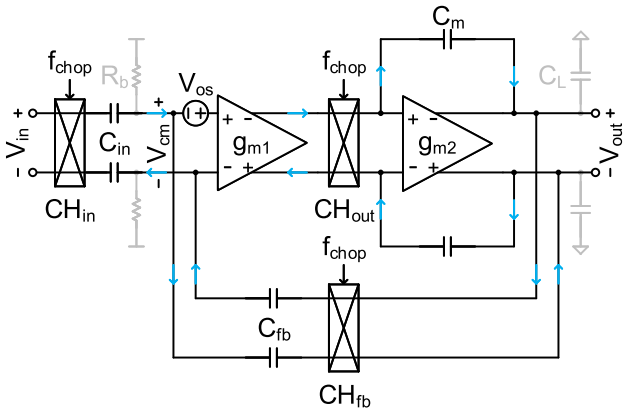


Fig. 1. A typical chopper-based instrumentation amplifier.

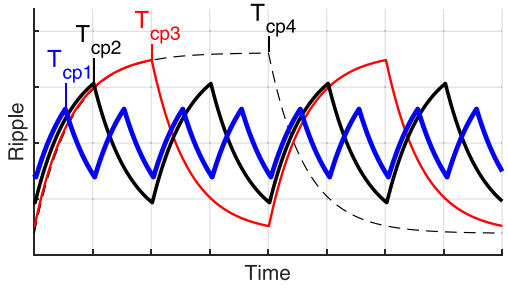


Fig. 2. Comparison of the ripple shapes of four different half chopping periods ($T_{cp1} < T_{cp2} < T_{cp3} < T_{cp4}$).

grounded and the Kirchhoff's current law (KCL) is applied to nodes $v_{cm+/-}$ and $v_{out+/-}$, namely

$$-v_{cm} \cdot sC_{in} = (v_{cm} + v_{out}) \cdot sC_{fb}, \tag{1}$$

$$(v_{cm} + V_{os}) \cdot g_{m1} = v_{out} \cdot sC_m. \tag{2}$$

After transforming (1), (2) into time-domain, the step responses of v_{cm} and v_{out} are

$$v_{cm}(t) = -V_{os} \cdot \left[1 - e^{-\left(\frac{g_{m1}}{C_m} \cdot \frac{C_{fb}}{C_{in}+C_{fb}}\right) \cdot t}\right], \tag{3}$$

$$v_{out}(t) = V_{os} \cdot \left(1 + \frac{C_{in}}{C_{fb}}\right) \cdot \left[1 - e^{-\left(\frac{g_{m1}}{C_m} \cdot \frac{C_{fb}}{C_{in}+C_{fb}}\right) \cdot t}\right]. \tag{4}$$

As expected, both v_{cm} and v_{out} exhibit RC-settling characteristics. When $t \to \infty$, v_{cm} settles to $-V_{os}$ to cancel out (compensate) the DC offset of the amplifier, which makes its input virtually short, while v_{out} settles to $V_{os} \cdot (1 + C_{in}/C_{fb})$, where C_{in}/C_{fb} is the signal gain of the IA by assuming a large open loop gain.

However, for an IA chopped at a frequency f_{chop}, the RC-settling process described by (3), (4) would be interrupted periodically for every period of $1/(2 \cdot f_{chop})$. As demonstrated in Fig. 2, a portion of the RC-settling process repeats every half chopping cycle, which results in the formation of different ripple shapes. Therefore, the shape and magnitude of the IA output ripple depend on the relation between the time constant

$$\tau_{IA} = \frac{C_m}{g_{m1}} \cdot \frac{C_{in}+C_{fb}}{C_{fb}} = \frac{C_m}{g_{m1}} \cdot \left(1 + \frac{C_{in}}{C_{fb}}\right), \tag{5}$$

and half of the chopping period

$$T_{cp} = \frac{1}{2 \cdot f_{chop}}. \tag{6}$$

Usually, in (5), the noise requirement of the IA determines g_{m1}, while the application requirement determines C_{in}/C_{fb}.

A. Triangular Ripple: $\tau_{IA} \gg 1/(2 \cdot f_{chop})$

When the time constant τ_{IA} is larger than half of the chopping period (T_{cp1} in Fig. 2), which happens if the Miller compensation capacitor C_m is large and/or when the chopping frequency is high, v_{out} only follows the settling process (4) for a very short period of time. Hence, the final ripple can be estimated by a linear approximation, which is

$$\frac{dv_{out}(t)}{dt} = V_{os} \cdot \left(\frac{g_{m1}}{C_m}\right) \cdot \left(e^{-t/\tau_{IA}}\right) \approx V_{os} \cdot \left(\frac{g_{m1}}{C_m}\right). \tag{7}$$

Within the half chopping period $1/(2 \cdot f_{chop})$, the peak-to-peak ripple voltage can be estimated as

$$V_{ripple\text{-}tri} = \frac{V_{os}}{2 \cdot f_{chop}} \cdot \frac{g_{m1}}{C_m}, \tag{8}$$

which is adopted in most of the literature about ripple estimation and mitigation [1], [6]–[8], [10]. A triangular ripple is obtained because the peak-to-peak ripple voltage is linearly proportional to g_{m1} and inversely proportional to f_{chop} and C_m. However, this estimation does not always hold true.

B. RC-Settling Ripple: $\tau_{IA} \approx 1/(2 \cdot f_{chop})$

When τ_{IA} is comparable to half of the chopping period (T_{cp2} and T_{cp3} in Fig. 2), the ripple shape appears as an RC-settling curve, which is also indicated by the output waveform in [6]. RC-settling ripple results when a low chopping frequency and/or a small Miller compensation capacitor are used. Depending on the ratio τ_{IA}/T_{cp}, the shape and magnitude of the output ripple vary and (8) is no longer accurate.

If the allowed settling time after chopping is long enough ($t \to \infty$), v_{out} would be settle to $V_{os} \cdot (1 + C_{in}/C_{fb})$ in the first half chopping cycle and $-V_{os} \cdot (1 + C_{in}/C_{fb})$ in the second half chopping cycle following the expression

$$v_{out}(t) = \pm V_{os} \cdot \left(1 + \frac{C_{in}}{C_{fb}}\right) \cdot \left(1 - e^{-t/\tau_{IA}}\right) + V_{int} \cdot e^{-t/\tau_{IA}}, \tag{9}$$

where V_{int} is the initial output voltage.

If the settling time of the system is only half of the chopping period (T_{cp}), the peak-to-peak ripple voltage can be expressed as the change of v_{out} during half of the chopping period by iterating $v_{out}(t + T_{cp})$ and $V_{int} = v_{out}(t)$, where

$$V_{ripple\text{-}RC} = 2 \cdot V_{os} \cdot \left(1 + \frac{C_{in}}{C_{fb}}\right) \cdot \frac{1 - e^{-\left(2 \cdot f_{chop} \cdot \tau_{IA}\right)^{-1}}}{1 + e^{-\left(2 \cdot f_{chop} \cdot \tau_{IA}\right)^{-1}}}. \tag{10}$$

This ripple shape is a segment of an RC-settled signal and varies with the ratio τ_{IA}/T_{cp}. An RC-settling ripple is obtained because the relationship between the output ripple, g_{m1}, f_{chop}, and C_m is non-linear.

C. Square Ripple: $\tau_{IA} \ll 1/(2 \cdot f_{chop})$

When τ_{IA} is much smaller than half of the chopping period, which happens in a high-speed IA and/or a low chopping frequency (T_{cp4} in Fig. 2), v_{out} can completely settle to $V_{\mathrm{os}} \cdot (1 + C_{\mathrm{in}}/C_{\mathrm{fb}})$ before another chopping event happens [11]. Thus, the output ripple is close to a square wave with a peak-to-peak amplitude of

$$V_{\text{ripple-sq}} = 2 \cdot V_{\mathrm{os}} \cdot \left(1 + \frac{C_{\mathrm{in}}}{C_{\mathrm{fb}}}\right). \tag{11}$$

This can also be derived by substituting $\tau_{\mathrm{IA}} \ll 1/(2 \cdot f_{\mathrm{chop}})$ into (10), which causes the two exponential terms to approach zero. A square ripple can thus be obtained and no matter how g_{m1}, f_{chop}, and C_{m} vary, the output ripple amplitude $V_{\text{ripple-sq}}$ will always remain the same.

D. Step-Change Ripple: $R_m \neq 1/g_{m2}$

Miller compensation uses a compensation capacitor C_{m} to perform "pole-splitting". By moving the first-stage pole towards the origin and the second-stage pole away from the origin, a larger phase margin can be ensured for stability [5]. However, the introduced right-half plane zero contributes an additional negative phase shift to the system. By placing a nulling resistor, which is usually equal to the inverse of the second-stage transconductance $R_{\mathrm{m}} = 1/g_{\mathrm{m2}}$, in series with the compensation capacitor, the right-half plane zero can then be eliminated or moved to the left-half plane. The literature suggested that instead of removing the zero, the size of the nulling resistance can be further increased to cancel out the non-dominant pole [12]. This technique works well in other amplifier typologies but results in a negative impact on the output ripple in CCIAs. Under this circumstance, the initial voltage described in (9) is displaced by an additional voltage step (illustrated in Fig. 4) when chopping swaps the positive and negative inputs. This is because of the imbalance between the compensation path and forward path when $R_{\mathrm{m}} \neq 1/g_{\mathrm{m2}}$.

To examine the instant behavior of the IA after a chopping event, the finite bandwidth of transconductance g_{m1} and g_{m2} is considered [10]. A refined model of the CCIA is shown in Fig. 3, which includes the output impedance R_{o1}, R_{o2}, and the nulling resistor R_{m}. The model is built by means of extending (1), (2), in which all intermediate node voltages have been considered. The compensation path and forward path of the second stage are also indicated. The expression of the output signal can be obtained using the following governing equations by applying KCL to every voltage node, namely

$$\begin{cases} v_{\mathrm{cm}} = -v_{\mathrm{out}} \cdot \dfrac{C_{\mathrm{fb}}}{C_{\mathrm{in}} + C_{\mathrm{fb}}}, v_{\mathrm{gm1}} = (v_{\mathrm{cm}} + V_{\mathrm{os}}) \cdot g_{\mathrm{m1}} R_{\mathrm{o1}} \\ v_{\mathrm{x}} = \dfrac{v_{\mathrm{gm1}} \cdot (R_{\mathrm{m}} + \dfrac{1}{sC_{\mathrm{m}}}) - v_{\mathrm{out}} \cdot R_{\mathrm{o1}}}{R_{\mathrm{m}} + R_{\mathrm{o1}} + \dfrac{1}{sC_{\mathrm{m}}}}, v_{\mathrm{gm2}} = v_{\mathrm{x}} \cdot g_{\mathrm{m2}} R_{\mathrm{o2}} \\ v_{\mathrm{out}} = \dfrac{v_{\mathrm{gm2}} - v_{\mathrm{cm}} \cdot sR_{\mathrm{o2}}C_{\mathrm{fb}} - v_{\mathrm{x}} \cdot \dfrac{sR_{\mathrm{o2}}C_{\mathrm{m}}}{sR_{\mathrm{m}}C_{\mathrm{m}} + 1}}{1 + sR_{\mathrm{o2}}C_{\mathrm{fb}} + \dfrac{sR_{\mathrm{o2}}C_{\mathrm{m}}}{sR_{\mathrm{m}}C_{\mathrm{m}} + 1}}, \end{cases} \tag{12}$$

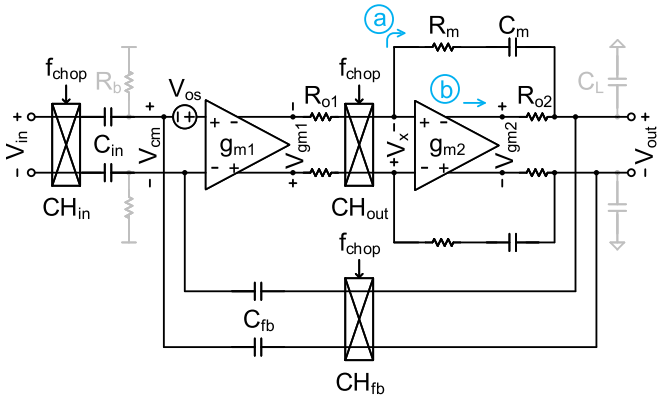


Fig. 3. Illustration of the two signal paths of the second-stage amplifier with nulling resistor (a) the compensation path via R_{m} and C_{m}, and (b) the forward path via the second-stage output impedance.

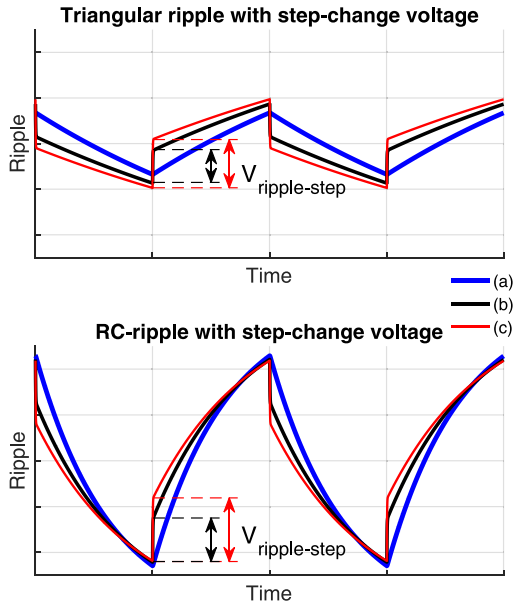
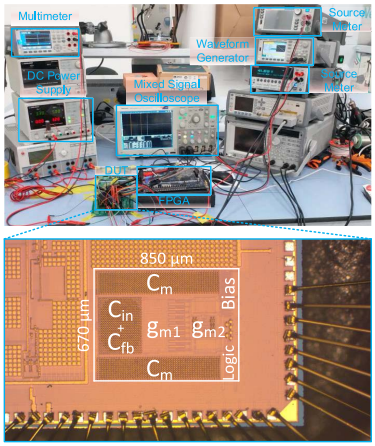


Fig. 4. Effect of the voltage step on triangular ripple and RC-ripple when (a) $R_{\mathrm{m}} = 1/g_{\mathrm{m2}}$, (b) $R_{\mathrm{m}} > 1/g_{\mathrm{m2}}$, and (c) $R_{\mathrm{m}} \gg 1/g_{\mathrm{m2}}$.

where v_{gm1} is the output voltage of g_{m1}, and v_{x} and v_{gm2} are the input and output voltages of g_{m2}, respectively. Transforming v_{out} into time-domain gives the exact form. For $g_{\mathrm{m1}}R_{\mathrm{o1}} \gg 1$ and $g_{\mathrm{m2}}R_{\mathrm{o2}} \gg 1$, the difference in v_{out} is negligible comparing to (4). The voltage step right after a chopping event is examined and can be simplified as

$$V_{\text{ripple-step}} = 2 \cdot V_{\mathrm{os}} \cdot \frac{\left(1 + \dfrac{C_{\mathrm{in}}}{C_{\mathrm{fb}}}\right) \cdot g_{\mathrm{m1}} \cdot \left(R_{\mathrm{m}} - \dfrac{1}{g_{\mathrm{m2}}}\right)}{\left(1 + \dfrac{C_{\mathrm{in}}}{C_{\mathrm{fb}}}\right) + g_{\mathrm{m1}} \cdot \left(R_{\mathrm{m}} - \dfrac{1}{g_{\mathrm{m2}}}\right)}. \tag{13}$$

Only when $R_{\mathrm{m}} = 1/g_{\mathrm{m2}}$ can this voltage step be null. Any other value of the nulling resistor R_{m} induces a step voltage, which is proportional to $R_{\mathrm{m}} - 1/g_{\mathrm{m2}}$. Note that this step-change voltage stacks on top of the initial output voltage V_{int} in (9). The voltage step has little impact on the voltage of the square ripple. For triangular ripple, however, such step significantly increases the resultant peak-to-peak ripple voltage. Even worse, the sharp change of the output ripple impairs the



g_{m1}	160 μS
R_{o1}	300 MΩ
g_{m2}	1 μS
R_{o2}	100 kΩ
C_{in}	20 pF
C_{fb}	0.2 pF
C_m	50 pF
R_m	1 MΩ
R_b	10 GΩ
f_{chop}	20 kHz

Fig. 5. Experimental setup for verifying the derived analytical model for ripple shapes/amplitudes and design parameters of the prototype chopper amplifier.

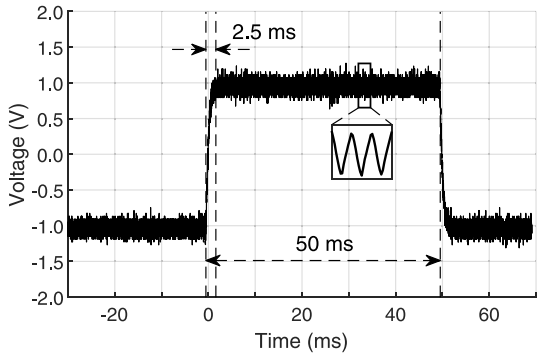


Fig. 6. Step response of the CCIA with a 10 mV input at 20 Hz.

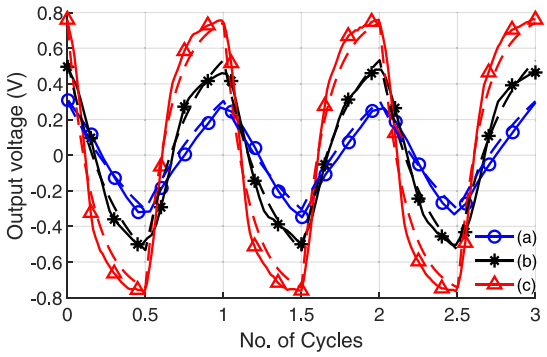


Fig. 7. Chip results (symbols) vs. MATLAB model (dotted lines) of different time constants and half chopping periods (a) $\tau_{IA} \gg 1/2 \cdot f_{chop}$, (b) $\tau_{IA} \approx 1/2 \cdot f_{chop}$, and (c) $\tau_{IA} \ll 1/2 \cdot f_{chop}$.

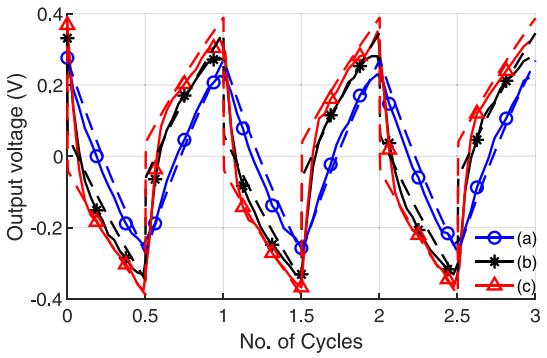


Fig. 8. Chip results (symbols) vs. MATLAB model (dotted lines) of different Miller compensation resistances and second stage transconductances (a) $R_m = 1/g_{m2}$, (b) $R_m > 1/g_{m2}$, and (c) $R_m \gg 1/g_{m2}$.

effectiveness of many feedback-based ripple-reduction techniques as the step-change voltage directly couples into the ripple-reduction loop, such as the one proposed in [1].

After Miller compensation, the non-dominant pole of the two-stage amplifier moves to $g_{m2}/(2\pi C_L)$, where C_L is the loading capacitor. It sets the lower bound of g_{m2} to ensure sufficient phase margin. Although a large loading capacitor burdens the second stage and increases current consumption, it actually smooths ripples and spikes because of its low-pass filtering characteristic [9], [10]. Note that the step-change ripple is also smoothed by the large loading capacitor, making it difficult to distinguish it from other types of ripple.

III. Silicon Verification

To validate the ripple analysis presented in Section II, a standard CCIA is realized in a 180 nm CMOS technology. An inverter-based cascode amplifier is adopted for the first stage with large input transistor sizing (30 μm/10 μm for PMOS and NMOS) to obtain a small intrinsic offset. The second stage is a standard common-source amplifier. Minimum-sized switches are implemented in all the choppers. Switched-capacitor common-mode feedback circuits are used to set the output common mode voltage of the two-stage amplifier (both first stage and second stage). The output loading is 4.5 pF. The feedback factor (β) of the CCIA is 1/100, which is set by the capacitor ratio C_{fb}/C_{in}. The two-stage structure gives an open-loop gain (A) of 130 dB. As a result, the closed-loop gain $[A/(1+\beta A)]$ of the CCIA is 40 dB and the loop-gain (βA) is 90 dB.

The testing setup is shown in Fig. 5. A 50 MHz FPGA board is used to generate clock signals for the device-under-test (DUT), which includes the 20 kHz chopping frequency (f_{chop}) as well. The input-referred noise of the CCIA is 80 $nV/\sqrt{\text{Hz}}$ with a noise corner of 0.25 Hz. The Noise Efficiency Factor (NEF) of the designed CCIA is 3.48 [1]. The Miller compensation capacitor is implemented as an array of unit capacitors with a set of selection switches to achieve size adjustment. The large biasing resistor (R_b) is realized by a 5 MΩ resistor with a 0.05% duty cycle 5 kHz signal to achieve an equivalent resistance of 10 GΩ [13].

The intrinsic offset of the DUT is determined at the beginning of the verification process. Inputs are provided to the DUT and the outputs are captured by the oscilloscope. As shown in Fig. 6, a triangular ripple is obtained at the output and the intrinsic offset is estimated to be 8 mV by (7). Then, the system time constant is decreased by reducing the Miller compensation capacitance. The waveform is compared with the MATLAB model using (9). The initial voltage is set to zero and 100 chopping cycles are provided for iteration until the system has reached its periodic steady state. Ripples obtained from three different Miller compensation capacitances (50 pF,

25 pF, 12.5 pF) are compared with the chip measurement results, which are indicated by the symbols in Fig. 7. Both waveforms show that the ripple shape changed gradually from a triangular ripple to an RC-settling ripple as τ_{IA} decreases along with the increase of C_{m}. The measured resultant ripple voltages also agree with the ripple voltage estimated by (10).

Since the prototype chopper amplifier is designed with $R_{\mathrm{m}} = 1/g_{\mathrm{m2}}$, it is set to be free of step-change ripple. When observing the step-change ripple derived in Section II-D, a 50 pF Miller compensation capacitor is used to obtain a triangular ripple. Then, the operation point of the second stage is varied to achieve three different g_{m2} settings (921.3 nS, 649.6 nS, 407.5 nS) by changing the input common-mode voltage (0.6 V, 0.54 V, 0.48 V). As shown in Fig. 8, the measurement results are compared with the model using (13). When a chopping event starts, a step-change voltage alternating in positive/negative directions is added to the initial output voltage. Then, the settling process begins. The resultant peak-to-peak ripple voltage is greatly increased compared to the triangular ripple, which further limits the output voltage swing. This step-change ripple can also be observed in the results presented in [8], [10]. However, there is no prior art that discusses and analyzes how such a ripple forms.

IV. Discussion

Ripple reduction techniques are discussed in state-of-the-art CCIA designs because offset-induced ripple always exists in CCIAs. Nevertheless, there is no comprehensive analysis of the shapes of CCIA ripples in [1], [6]–[8], [10]. Misconceptions about ripple formation can often lead to an over-design in component sizing and a lower ripple reduction effectiveness. This brief is the first attempt to categorize ripples into four different shapes instead of just the triangular shape. Thoroughly analyzing ripple formation before the design of a CCIA is crucial to the effectiveness of the ripple reduction techniques applied.

Many CCIA designs tend to use a large capacitor for Miller compensation because (8) stated that the magnitude of the triangular ripple is inversely proportional to the Miller compensation capacitor. However, as discussed in Section II, a smaller compensation capacitor results in a smaller time constant and changes the ripple shape. The dependence of ripple magnitude on compensation capacitor is strong in triangular ripple and diminishes from RC-settling ripple (10) to square ripple (11). Thus, reducing ripple by a larger Miller compensation capacitor is not a cost-effective approach, not only because the reduction is insignificant ($\sim$6 dB) compared to the ripple reduction loop ($>$45 dB [1]) and the notch filtering ($>$54 dB [7]), but also because the expense of the chip area for the capacitor is huge and the system bandwidth is slower.

Some designs use a larger nulling resistor to secure more system phase margin. However, it is an inappropriate approach for triangular ripples because it will introduce an extra voltage step. This step could directly couple into the capacitor-coupling-based ripple-reduction loop and degrades its performance [1], [6]. Ripple reductions performed before the second stage (notch-filtering [7], high-pass filtering [8], [10], etc.) cannot deal with step-change ripple as well because it comes from the imbalance between R_{m} and $1/g_{\mathrm{m2}}$. Thus, as analyzed in Section II-D, a good matching between the Miller nulling resistor and the second-stage transconductance is crucial to minimize the step-change ripple.

V. Conclusion

This brief has analyzed the formation and shape of the output ripple in a chopper-based instrumentation amplifier. The dependency of the ripple is quantified based on five major design parameters, according to which the shape of the output ripple can be classified into three types. A fourth type is induced by varying the size of the nulling resistor of the Miller compensation. Based on the findings, the impact of different ripple shapes on the effectiveness of the ripple reduction techniques has been analyzed. The derived ripple model is validated with silicon results. This analysis can serve as a guideline for high-performance chopper-based amplifier designs and is especially useful for ripple-reduction schemes.

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