An Asynchronous CMOS Current Readout With 124-dB Dynamic Range for Bioluminescence Sensing

Muhammad Asfandyar Awan, Khalil Ahmad, Amine Bermak, Kabir H. Biswas, and Bo Wang, *Senior Member, IEEE*

***Abstract*—This letter presents a photocurrent readout for bioluminescence detection. The design incorporates an asynchronous architecture employing a proposed capacitive feedback transimpedance amplifier (C-TIA) with a self-timed reset network and an all-digital reconfigurable time-domain quantization scheme. It eliminates the need for a periodic reset signal required in conventional C-TIAs and offers a wide dynamic range (DR) of 124 dB, a nonlinearity of 1.7%, and a 1-pArms input-referred noise while drawing only 210 μA from a 1.8-V supply. Fabricated in a standard 180-nm CMOS technology, it occupies an area of 0.16 mm^2. This design aims to facilitate in vitro NanoLuc (NLuc) luciferase-based bioluminescence sensing for biomolecule quantification at room temperature, with preliminary biological testing presented in this letter.**

***Index Terms*—Bioluminescence sensing, current readout, high dynamic range, low noise.**

I. Introduction

There is a pressing need to revolutionize the healthcare industry by facilitating the development of robust, low-cost, and integrated diagnostic technologies, and integrating a CMOS chip into diagnostic devices is promising in achieving this goal. By offering high sensitivity and great specificity, affinity-based bioluminescence detection is the most widely used and highly effective approach in diagnostics [1]. This work focuses on developing a current readout interface for NanoLuc (NLuc) luciferase-based bioluminescence sensing to quantify biomolecules and to detect pathogens, proteins, and DNA sequences [2]. In such applications, luciferase enzyme-based reactions exhibit a photoemission rate ranging from 10^4 photon/s to 10×10^8 photon/s, mandating a readout above 100-dB dynamic range (DR). Meanwhile, due to the exponential decay property of bioluminescence, a high-speed readout (e.g., μs$\sim$ms) is required at high intensity to capture its transient details, while a low noise (e.g., pA-level) readout is desired to sense the bioluminescence strength at the plateau [3], [4].

A typical current readout includes a transimpedance amplifier (TIA) with resistive or capacitive feedback [5], [6], [8], [9], followed by an analog-to-digital converter. However, few designs have achieved a pA-level resolution while maintaining a wide DR. Marefat et al. [11] presented a light-to-digital converter using an active integrator that achieves a DR of 108 dB while employing an explicit DAC and an integrated digital signal processing unit for DR extension. Lin et al. [12] achieved 119-dB DR using a capacitive feedback TIA (C-TIA), where its minimum detectable current is 200 pA limited by the noise from its dc servo loop and the 7-bit I-DAC in its feedback. In [13], an even larger DR up to 160 dB is achieved with an asynchronous current-mode $\Sigma\Delta$ ADC readout, but requiring an off-chip predictive DAC along with an expensive fifth-order polynomial calibration for DR extension and linearity correction, respectively, making it both area- and power-hungry. This design breaks the DR, noise, and power consumption tradeoff with an asynchronous architecture comprising a self-reset C-TIA to accommodate a wide input range while maintaining the linearity and adopting a time-domain comparator for noise and offset averaging. This readout is particularly suitable for bioluminescence readouts with different speed requirements at different signal strengths.

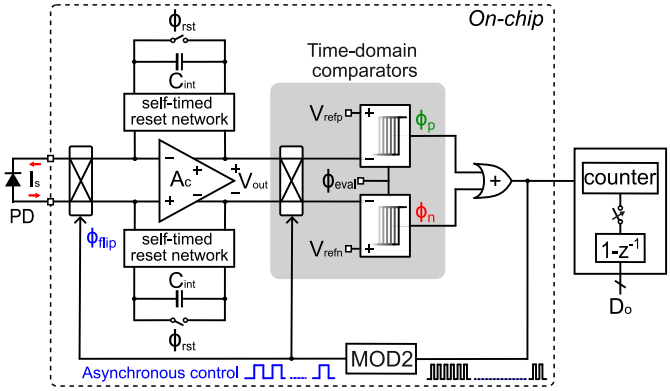

Fig. 1. Block diagram of the proposed current readout.

II. System Architecture

The proposed differential asynchronous current readout is shown in Fig. 1. It consists of a C-TIA with an asynchronous flip switch at the input, two reconfigurable time-domain all-digital comparators, and a digital counter. Outputs of the two comparators are XOR-ed to generate the required control of the asynchronous C-TIA input/output flip switch. A differential readout was implemented mainly to mitigate common mode noise, ensure balanced sensor impedance at differential inputs, and extend the DR by 6 dB compared to a single-ended one [7]. Furthermore, the photodiode is configured in the photovoltaic mode of operation, eliminating the need for a voltage biasing [7], [8]. The following will present the proposed system operation, highlighting the merits of the asynchronous architecture.

A. Photocurrent to Frequency Conversion

Conventional C-TIA with periodic reset can integrate the input current I_s if it is within the maximum input range $I_{s,\max}$. As demonstrated in Fig. 2(a), if I_s exceeds $I_{s,\max}$, the integrator will saturate and the C-TIA cannot operate until the next reset occurs, which is addressed in the proposed design. As shown in Fig. 2(b), a reset is applied before each conversion, and the differential C-TIA output V_{out} is set to zero. Subsequently, the C-TIA integrates the

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Muhammad Asfandyar Awan, Khalil Ahmad, Amine Bermak, and Bo Wang are with the College of Science and Engineering, Hamad Bin Khalifa University, Doha, Qatar (e-mail: bwang@hbku.edu.qa).

Kabir H. Biswas is with the College of Health and Life Sciences, Hamad Bin Khalifa University, Doha, Qatar.

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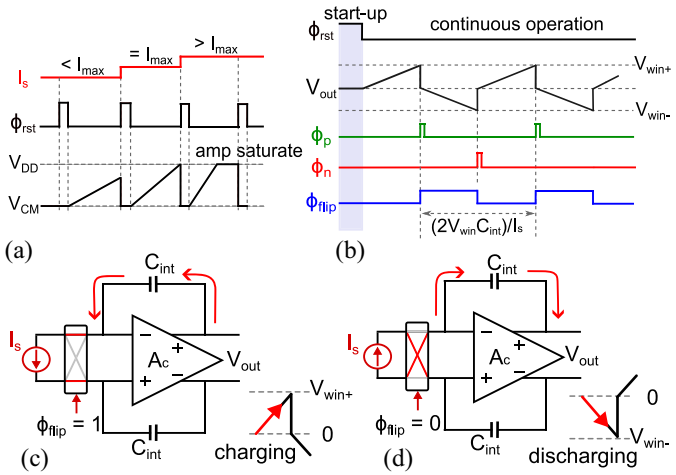

Fig. 2. (a) Waveform of a conventional C-TIA with periodic reset. (b) Simplified timing diagram of the proposed current readout. C-TIA with asynchronous flip switch folds V_{out} by charging and discharging C_{int} alternatively in (c) and (d), respectively.

input I_s. Its output V_{out} is bounded within a predefined voltage window V_{win} by the two time-domain comparators. As a result, V_{out} undergoes asynchronous folding, resulting in current-to-frequency (I-to-F) conversion. The polarity of I_s, as controlled by ϕ_{flip}, is flipped asynchronously at a speed of $I_s/(2 \cdot V_{\text{win}} \cdot C_{\text{int}})$, which is proportional to the magnitude of I_s. With this, the C-TIA will continue to integrate I_s by charging [Fig. 2(c)] or discharging [Fig. 2(d)] C_{int} according to the polarity of the input, without experiencing the saturation issue as in a conventional C-TIA.

B. Improved Dynamic Range

Implementing the asynchronous flip switch at the input of the C-TIA will eliminate the need for a periodic reset switch required in the feedback of a conventional C-TIA. Therefore, it can achieve continuous-time operation with a higher DR than conventional C-TIAs and can handle large input currents. As a result, the bandwidth of the system is not limited by the speed of a master system reset clock. Meanwhile, this C-TIA samples the input current I_s asynchronously rather than adhering to a fixed clock rate, enabling varied sampling speed to capture both accurate decaying profile at high bioluminescence intensity and precise bioluminescence intensity quantification when it is weak.

This design does not limit the minimum detectable input signal by a predetermined integration time [12]. At the same time, the maximum allowed input is not limited by the output range of the output of a feedback current DAC [2], nor does it require an explicit DR extension loop [13]. Furthermore, using a large feedback capacitor C_{int} (i.e., 4 pF) also contributes to higher DR by maintaining a reasonable switching frequency to control the synchronous switch at the C-TIA input.

C. Self-Timed Capacitor Reset Network

The occurrence of input switching (i.e., ϕ_{flip} changes) can cause reset transients (i.e., an over/undershot in V_{out} of the C-TIA), thus altering the period of ϕ_{flip}. To address the issue, a self-timed switched capacitor reset network, shown in Fig. 3, is proposed to minimize reset/flip transients. Two complementary control signals ϕ_{flip} and $\overline{\phi}_{\text{flip}}$ toggles the active integration capacitor from two pairs of matched capacitor banks, C_{p1} and C_{n1} or C_{p2} and C_{n2}. Thus, only one capacitor pair is active at any moment while the other is

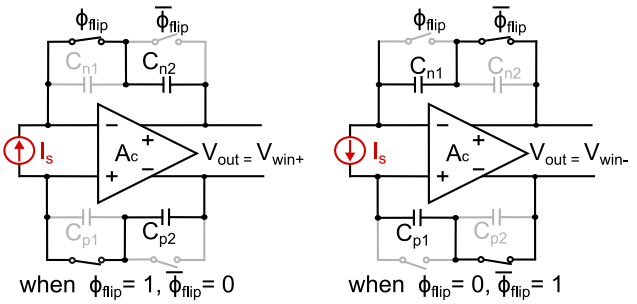

Fig. 3. Proposed self-timed switched capacitor reset network.

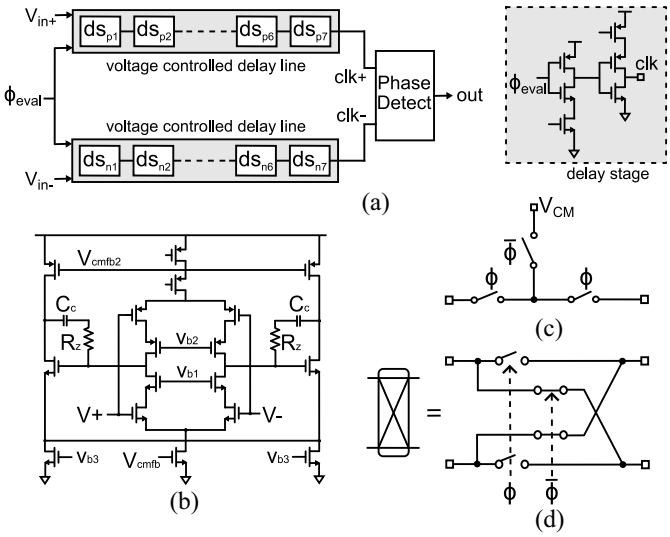

Fig. 4. Implementation of (a) time-domain comparator, (b) current reuse amplifier, (c) low-leakage reset switch, and (d) C-TIA input flip switch.

reset. Importantly, all capacitors $C_{n1/2}$,$C_{p1/2}$ in the reset network are locally charged balanced, that is, without the current supplied from the core amplifier A_c. With this arrangement, V_{out} has a constant trip of $V_{\text{win+/-}}$, thus the period of ϕ_{flip} remains consistent corresponding to the input current.

III. Circuit Implementation

This section describes the main building blocks' circuit implementation and design considerations, including the time-domain comparator, integrator amplifier, and low-leakage switches implemented for the readout.

A. Time-Domain Comparator

A 7-stage reconfigurable time-domain comparator (RTDC) is adopted in this design [14]. As shown in Fig. 4(a), it consists of two voltage-controlled delay lines (VCDLs) and a phase detector (PD). Running at an evaluation clock ϕ_{eval} of 12.5 MHz, the RTDC achieves 4× better power efficiency (i.e., 14 μA) with the benefit of noise averaging compared to a classical continuous-time comparator (i.e., 56 μA) with the same speed. The input referred noise and the offset of the RTDC are attenuated by a factor of $\sqrt{2N}$, where N is the number of active delay stages in the delay line [14]. The PD compares the phase difference between the two output signals from the VCDLs and generates the comparison result. The power consumption of the inverters in the delay stages, as shown in Fig. 4(a), dominates the overall power of the comparator.

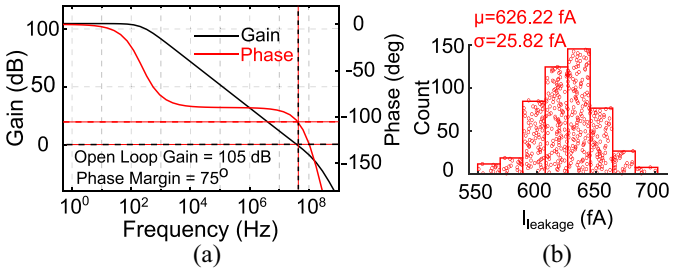

Fig. 5. Post-layout simulation results of the (a) implemented integrator amplifier A_c and (b) low-leakage reset switch.

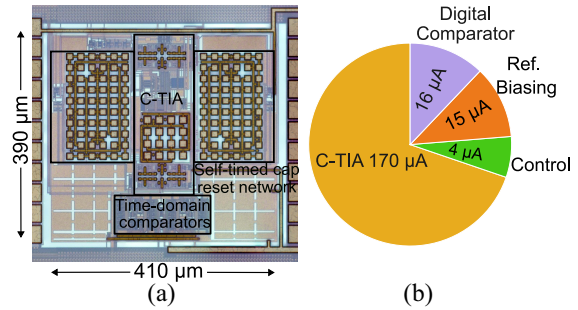

Fig. 6. (a) Chip micrograph. (b) Readout power distribution.

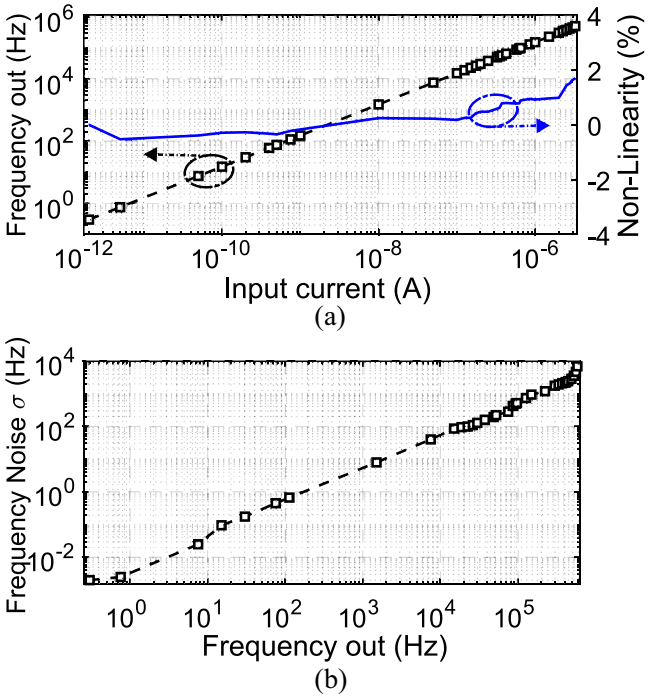

Fig. 7. (a) Measured ϕ_{flip} and corresponding linearity versus the input current. (b) Noise at different frequency outputs.

B. Integrator Amplifier

An amplifier with sufficiently high transconductance and gain is required to ensure accurate charge transfer while consuming minimum current. The gain of the amplifier will attenuate noise from subsequent blocks. This design employs a two-stage current-reused amplifier topology, as shown in Fig. 4(b). Fig. 5(a) shows the OTA simulation results, which have a dc gain of 105 dB and 35-MHz UGBW, assuming an input photodiode parasitic capacitance of 10 pF, and a $C_{n1/2}$, $C_{p1/2}$ of 4 pF each in the self-timed capacitor reset network.

C. Low-Leakage Switch

Before the integration begins, both the input and output nodes of the C-TIA are reset to V_{CM}. Once the integration of I_s starts, the reset switch is turned off. Since the reset switch is off during conversion for a significant amount of time, particularly at weak bioluminescence conditions, a low-leakage switch (< 700 fA in RT) shown in Fig. 4(c) is therefore mandatory to avoid the integrator linearity degradation. Fig. 5(b) shows the simulation results of the input node of the C-TIA, exhibiting an off-state leakage current ≤ 1 pA at room temperature. Fig. 4(d) depicts the implementation of the asynchronous flip switch, where the transistors are minimum size to minimize charge injection during the capacitor reset.

IV. Measurement Results

The chip microphotograph is shown in Fig. 6(a), occupying an area of 0.16 mm^2 fabricated in a standard 0.18-μm CMOS process. Fig. 6(b) shows the power consumption distribution of the major building blocks (210 μA total from a 1.8-V supply). The readout common mode voltage is 900 mV, while the window reference voltages $V_{\text{refn/p}}$ are 500 mV and 1.3 V, respectively. Fig. 7(a) illustrates the measured output and the corresponding nonlinearity for an input range of 2 pA–3.25 μA, corresponding to a DR of 124 dB and a conversion time of 3.3 s to 1.90 μs, respectively. The minimum detectable current is limited by circuit noise, whereas the integrator bandwidth limits the maximum input range. Fig. 7(b) shows that the measured frequency noise standard deviation is 0.560, 1.374, and 3.5 kHz at output frequencies of 100 kHz, 253 kHz, and 525 kHz, respectively. This shows an improvement of 11% compared to the frequency noise performance reported in [15] while only

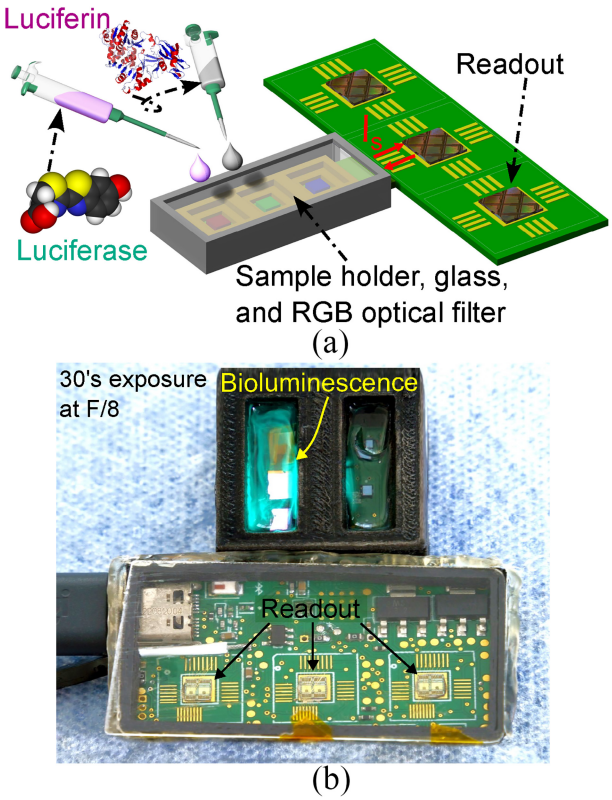

Fig. 8. (a) Illustration of bioluminescence testing setup. (b) Prototyped bioluminescence system using the designed chip.

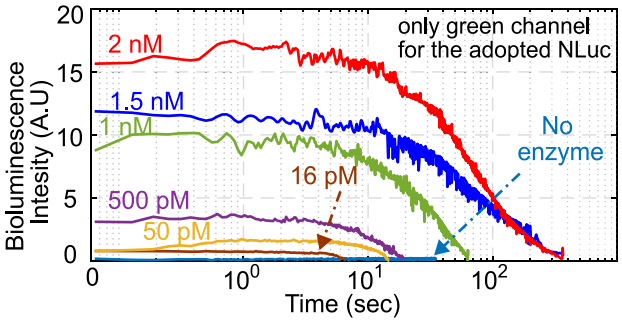

Fig. 9. Measured bioluminescence intensity and time decay profile, using N-Luc cells with seven different concentrations from 0 to 2 nM.

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART DESIGNS

References	[6]	[11]	[12]	[13]	[16]	This Work
Architecture	TIA + ADC	LDC I-ΣΔM	Dual-slope	Asynchronous ΣΔ	ΣΔ + SAR	Asynchronous I-to-F
Technology(nm)	180	180	180	180	55	**180**
Supply (V)	1.8	1.5/2.5	1.2	1.8	1.2	**1.8**
Area (mm^2)	9	2.6	-	0.5	0.585	**0.16**
Noise (pA_{rms})	260	-	100	0.14	-	**1**
Max input (μA)	40	25.6	200	10	200	**3.25**
DR extension scheme	Ext. Current source	DAC + DSP	DC Servo Loop	Predective DAC	-	**None**
Conversion time (ms)	-	0.128	-	0.0032 ~ 3200	2	**0.0019 ~ 3300**
Dynamic Range (dB)	102	108.2	119	160	127	**124**
Nonlinearity (%)	-	-	-	0.07*	0.0826*	**1.7**
Power (uW)	460	280	196	295†	1011	**378**

* high-order polynominal fitting for linearity correction

† power consumption of the predictive DAC and linearity correction not included

burning one-ninth of its current. Fig. 8(a) and (b) shows the prototype bioluminescence detection system using the designed readout and the test setup. Multiple concentrations of cell lysate were tested, and the observed decay profile and detected intensity (shown in Fig. 9) were aligned with the findings reported in [3] and the Promega GloMax laboratory instrument. Specifically, the pM-level detection limit is comparable to the instrument with a detection limit of 10 pM under the same setup, demonstrating the sensitivity of the design. The performance of the designed current readout is compared with the state of the art listed in Table I. The proposed architecture has achieved a wide DR of 124 dB and maintains linearity up to 98.3% with constant biasing. It does not require an additional feedback loop for the DR extension and current scaling or high-order polynomial fitting for linearity correction.

V. CONCLUSION

This letter describes a current readout that eliminates the need for an external reset and a sampling clock, thereby removing the constraint of a predetermined sampling rate as in conventional current-to-frequency converters. Furthermore, this design expands the DR without requiring a feedback loop or explicit DAC. A prototype bioluminescence sensing system that utilizes the designed high DR readout can accurately capture the bioluminescence intensity and overall decay time, making it a promising device for rapid diagnostics.

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